A SEQUENTIAL PULSE GENERATOR FOR THE THYRISTOR CONTROL OF INDUCTION MACHINES AND REVERSIBLE RECTIFIERS

by

MICHAEL D. BROWN, B.Sc.

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SUMMARY

Momentary device conduction such as occurs in diodes during reverse recovery renders application of thyristor anode holding current difficult in some inverter circuits. Application of gate holding current renders anode holding unnecessary.

3-layer transistors may be used in the generation of thyristor gate firing signals of high quality.

Circuits are described in which thyristor gate firing pulses and gate holding pulses are generated digitally, using 3-layer active devices. The particular application is for control of a double 3-phase bridge inverter with ring-of-3 commutation, but the principles used are applicable to other inverter types.

Frequency control is provided with synchronous running by phaselock loop. Control ranges are from zero frequency to any useful inversion frequency and 315 degrees in output phase, with control by proportional d.c. analogue in both cases.

Versatility is illustrated by use of the pulse generator in the control of a thyristor frequency changer, and in the control of a circuit in which 3-layer devices are used to simulate 4-layer devices, to separate phenomena encountered in inverter research.

LIST OF CONTENTS

CHAPTER 1

INTRODUCTION

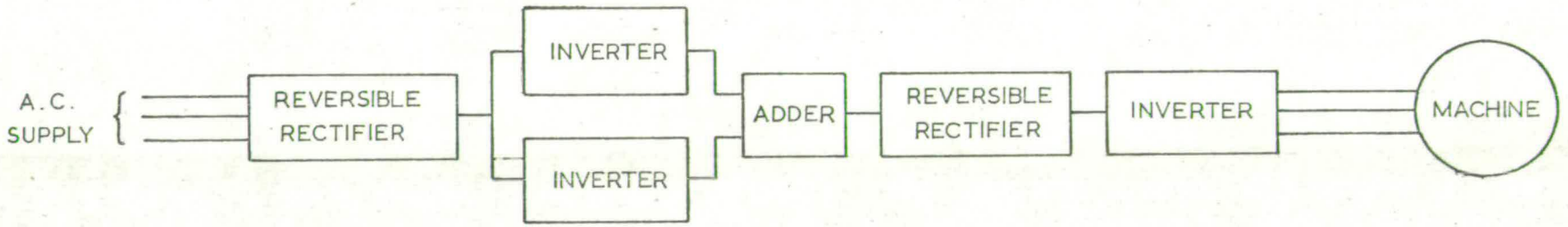
This work is related to variable frequency control of induction machines, and to reversible rectifiers in which direct current may flow in either direction.

Both applications may use the same thyristor-inverter configuration and the same sequential-logic system; otherwise the induction motor requires a pulse generator with frequency control whereas the reversible rectifier requires a pulse generator with synchronised frequency and phase control.

Fig. 1 shows a scheme proposed to feed an a.c. machine at variable frequency and variable voltage from a supply with fixed frequency and fixed voltage using thyristor inverters. Operation of reversible rectifier A at the maximum voltage ensures high power factor operation on the supply side, and minimum waveform distortion on both sides. The outputs from inverters B with controlled phase relationship are added and rectified at D to feed variable direct voltage to inverter E. This unit feeds the motor at variable frequency. B may operate at a high frequency to minimise iron cross-sections; this frequency is constant and voltage control in A is unnecessary.

1.1 Thyristors

The name thyristor defines any semiconductor switch whose bistable action depends on p-n-p-n regenerative feedback. Thyristors can be 2, 3 or 4-terminal devices, and both unidirectional and bidirectional types are available.


A.C.
SUPPLY
REVERSIBLE
RECTIFIER
INVERTER
INVERTER
ADDER
REVERSIBLE
RECTIFIER
INVERTER
MACHINE

Classification of Thyristors

Types of thyristor currently available include the following:

1. silicon controlled rectifier
2. silicon unilateral switch
3. light activated silicon controlled rectifier
4. gate turn-off switch
5. silicon controlled switch
6. Shockley diode
7. triac
8. silicon bidirectional switch

Types 1 to 6 are unidirectional thyristors and can conduct in one direction only; types 7 and 8 are bidirectional and can carry current in either direction. Types 1, 3, 4 and 7 each have one control electrode (gate) which can be used to initiate conduction in the anode circuit; the gate of type 4 can also be used to turn the device off. Light may be used to initiate conduction in type 3, the gate being used as a sensitivity control if required; types 6 and 8 have no control electrode, type 5 has two.

"Thyristor" henceforward means silicon controlled rectifier, except where context shows the more general meaning to be in use.

1.1.1 Construction

The most popular methods of construction of the p-n-p-n semiconductor pellet are:

1. diffused
2. alloy diffused
3. planar diffused

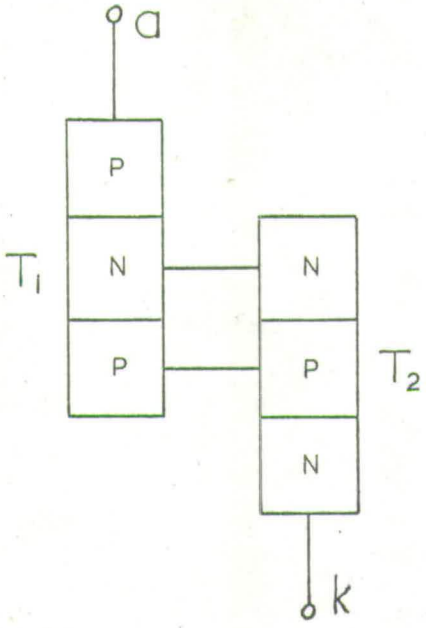
Construction of types 1 and 2 starts with diffusion of p-type impurities into both sides of a wafer of n-type silicon. The final n-type layer is then either diffused through a mask (type-1) or in the case of large thyristors a gold-antimony pellet is fused into the p-n-p pellet to furnish the final n-type layer (type-2). The latter process in both types leaves space if needed for an external gate connection to the n-type layer which is sandwiched between two p-type layers. Similar techniques are used to produce the more complex types such as triacs.

In planar structures, successive diffusions are made through suitable masks so that access to several layers is from one side of the pellet; silicon oxide can be used to seal all external faces and thus give surface protection, but current carrying capacity is poor for the amount of silicon used.

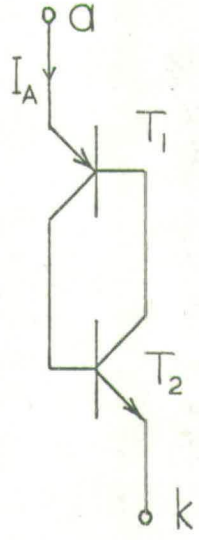
The semiconductor pellet is soldered, hard soldered or held in compression to a heat conducting base; this may be attached to a heat sink for cooling. Encapsulation with hermetic sealing is required for alloy diffused thyristors; planar thyristors do not need hermetic sealing and are usually small devices protected by a moulded plastic case.

1.1.2 Two Transistor Analogy of p-n-p-n Operation

In Fig. 1.1.2 (a) the p-n-p-n thyristor structure is shown divided into two components which each have the structure of a transistor. Conductors join the transistors so as to retain the original contacts, giving the equivalent transistor circuit of Fig. 1.1.2 (b).



1.1.2(a)



1.1.2(b)

The common emitter current gain h_{FE} of each transistor has a low value at small emitter currents and a higher value at larger collector currents. At low emitter currents, h_{FE} of T_1 x h_{FE} of T_2 is less than unity and the device is stable. Increase of emitter current in one of the transistors raises the product of the current gains to unity; this makes further increase of current automatic, and the device turns on.

The increase of emitter current can be brought about by:

1. high voltage
2. high rate of change of voltage
3. high temperature
4. light
5. transistor action

Method 1 depends on avalanche breakdown in a reverse blocking semiconductor junction, method 2 depends on current charging the device capacitance. Method 3 depends on the rise of leakage current with temperature in a semiconductor, and method 4 depends on the rise of leakage current caused by absorption of radiant energy within the spectral bandwidth of silicon. In method 5, current is applied directly to one of the intermediate layers, corresponding to the base of one of the transistors.

1.1.3 Shorted Emitter Thyristor

An internal short circuit between the gate and cathode of a thyristor remote from the gate lead diverts some of the device leakage current from the gate-cathode junction without unduly reducing gate sensitivity. This enables a thyristor to withstand high values of dv/dt and high temperatures.

1.1.4 V-I Characteristics of Reverse Blocking Thyristors

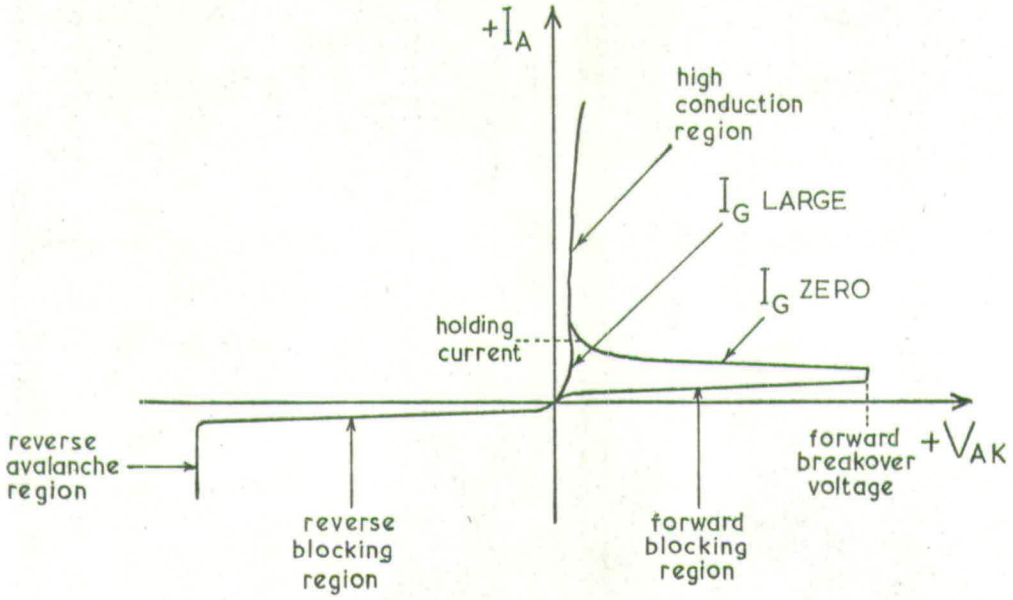
Fig. 1.1.4 shows the V-I characteristics of a reverse blocking thyristor. In the forward blocking region, ~~increase of~~ forward breakover voltage is reached, when avalanche multiplication takes place. Increase of current to the point at which internal loop gain (transistor analogy) becomes unity results in the device switching into the high conductivity region. Reduction of anode current below the holding value results in the device reverting to the forward blocking state. In the reverse direction, two p-n junctions in series are both reverse biased, so the characteristic is that of a p-n junction diode.

For increasing values of gate current, the forward breakover voltage is reduced; a high value of gate current results in complete removal of the forward blocking region, making the anode-cathode V-I characteristic similar to that of a p-n junction diode.

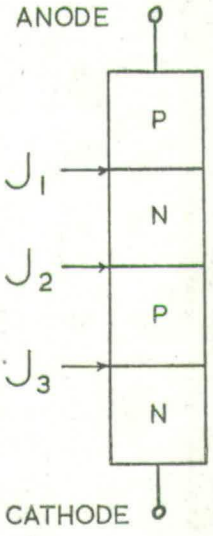
1.1.5 Reverse Blocking Thyristor Turn-off Mechanism

When a reverse blocking thyristor is in the conducting state, each of the junctions of Fig. 1.1.5 is in a condition of forward bias. Recovery of blocking capability of the junctions is initiated by reduction of anode current to zero, and reverse anode current shortens recovery time of junctions J_1 and J_3. When J_1 and J_3 regain blocking capability, reverse voltage may be applied to the thyristor.

Forward blocking depends on junction J_2; recovery time of this junction is long compared with J_1 and J_3, and cannot be shortened by application of current to the electrodes.


+I_A
high conduction region
I_G LARGE
I_G ZERO
holding current
reverse avalanche region
reverse blocking region
forward blocking region
forward breakover voltage
+V_AK

1.1.4


ANODE
P
J1
N
J2
P
J3
N
CATHODE

1.1.5

During the greater part of the recovery of J_1 and J_3 the anode-cathode voltage is about + 0.7 V.

1.1.6 Comparison of Thyristors with other Semiconductors

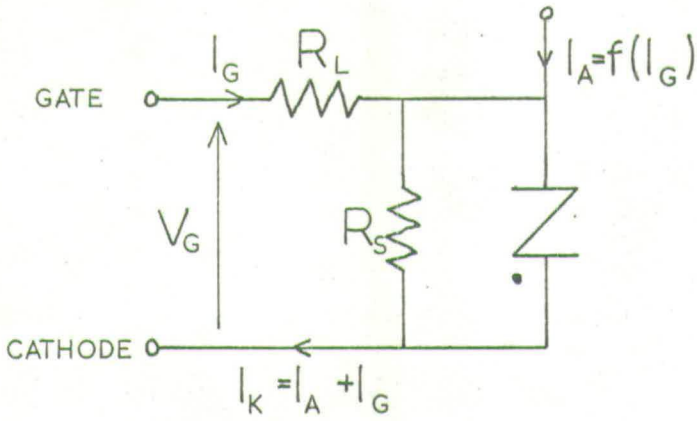
An ordinary 3-layer transistor has a narrow base region to maximise h_{FE} at low currents. A thyristor must have low values of h_{FE} at low currents, so the base region is made wide; this is compatible with high voltage operation, making the thyristor a high voltage device, and it is easier to manufacture with a given accuracy than a narrow base region.

1.2 Gate Input Characteristics of Thyristors

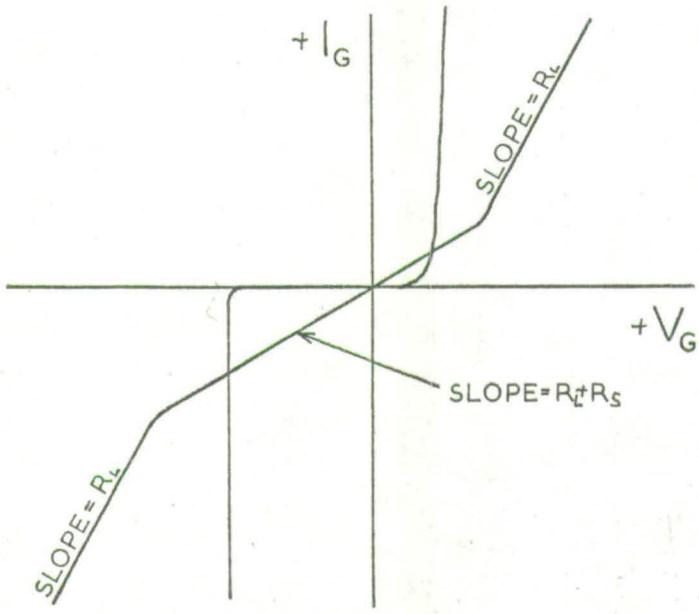
Fig. 1.2 shows the low-frequency equivalent circuit of a thyristor gate-cathode junction at (a), and the input v-i charcteristic at (b). R_L represents the lateral resistance of the p-type semiconductor layer to which the gate terminal is connected and R_S represents the effect of an emitter short circuit.

When increasing forward gate current is applied to a thyristor with the anode supply connected, anode current rises, reducing the gate input current (region A-B, Fig. 1.2(c)). At point B, the slopes of the gate input and source V-I characteristics become equal, and further increase of source current results in the source V-I characteristic leaving the gate input characteristic for $I_a = f(I_G)$, as the thyristor turns on. I_{GT} is the minimum current required to trigger the thyristor and V_{GT} the minimum voltage; the latter depends on source impedance, as its derivation in Fig. 1.2(c) shows.

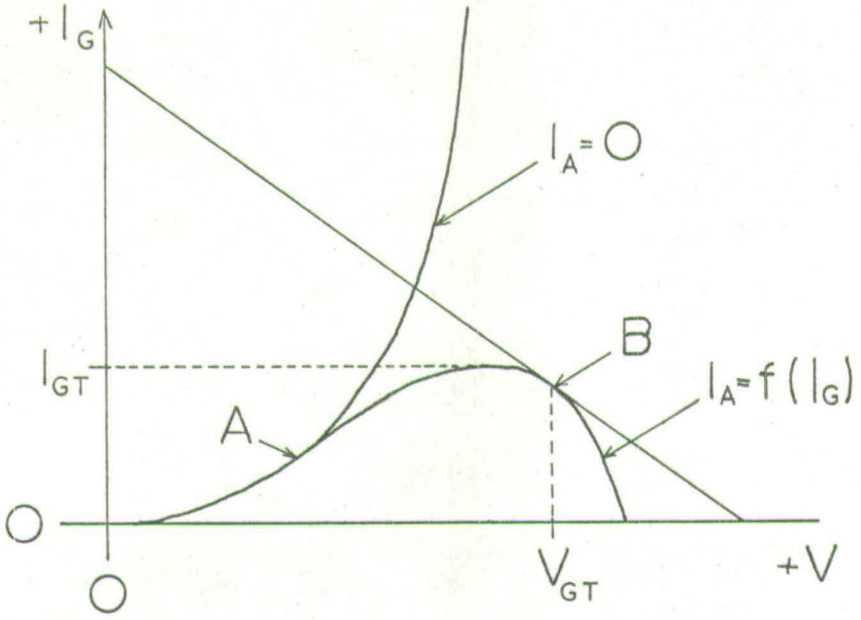
With anode current above the holding value, the gate-cathode junction becomes a source, Fig.1.2(d) having open-circuit voltage nearly equal to the anode-cathode voltage drop, and internal


GATE
I_G
R_L
$I_A = f(I_G)$
V_G
R_S
CATHODE
$I_K = I_A + I_G$

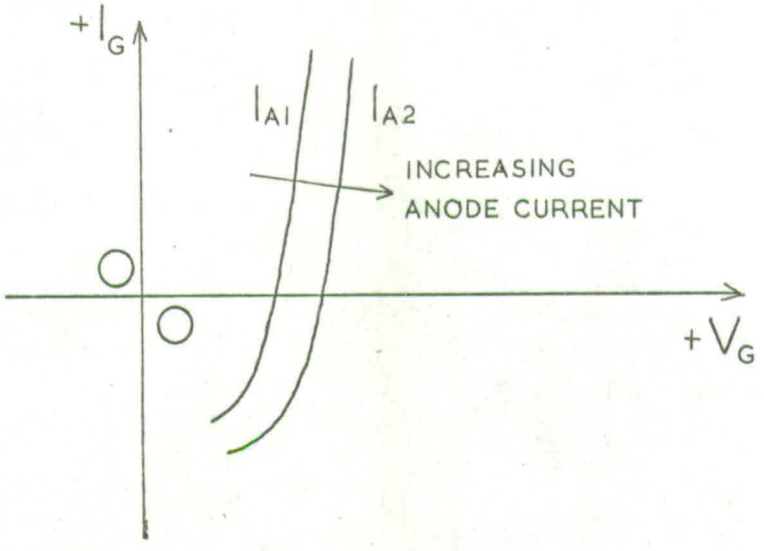
1.2(a)


$+I_G$
SLOPE = R_L
$+V_G$
SLOPE = $R_L + R_S$
SLOPE = R_L

1.2(b)


+ I G
I A = O
B
I GT
I A = f (I G)
A
O
O
V GT
+V

1.2(c)


+ I G
I A1
I A2
INCREASING
ANODE CURRENT
O
O
+ V G

1.2(d)

impedance R_L. The curvature in the fourth quadrant is due to the effect of reverse gate current on the distribution of anode current within the device.

1.2.1 Effects of Gate-Cathode Impedance and Bias

External shunt resistance applied to thyristors having low R_L and high R_S (not shorted emitter types) reduces the regenerative action of the thyristor. This raises the latching and holding current and forward breakover voltage and dv/dt withstand capability, and reduces turn-off time by recovering stored charge and by its effects on latching and holding current.

Shunt capacitance can reduce the sensitivity of a thyristor to dv/dt, without loss of sensitivity to D.C. gate signals. It also retards the rate of rise of gate voltage and this in turn retards the rate of rise of anode current at turn-on. It also maintains gate voltage during the turn-off period, lengthening turn-off time and raising reverse leakage current.

Capacitance in series with the gate source can impose reverse gate voltage at the end of a firing pulse, momentarily raising the holding current requirement.

Inductance between gate and cathode reduces sensitivity to slow changes of anode current or gate source current, giving improved thermal stability. With anode current flowing, reverse gate current builds up in the inductance; this raises the holding current requirement by as much as 10:1, and increases dv/dt rating.

A parallel resonant circuit connected between gate and cathode can produce a condition of oscillation. With the thyristor conducting, negative gate current builds up in the inductor, increasing the holding current; if the anode current is less than this, the thyristor will turn off. Current from the inductance then flows through the capacitor, in a resonant manner. When gate voltage (= capacitor voltage) swings positive again, the thyristor will turn on.

Positive gate current increases leakage current with the anode negative; the effect on cooling requirements is negligible for $|-V_G|$ less than $\frac{1}{4}$ V.

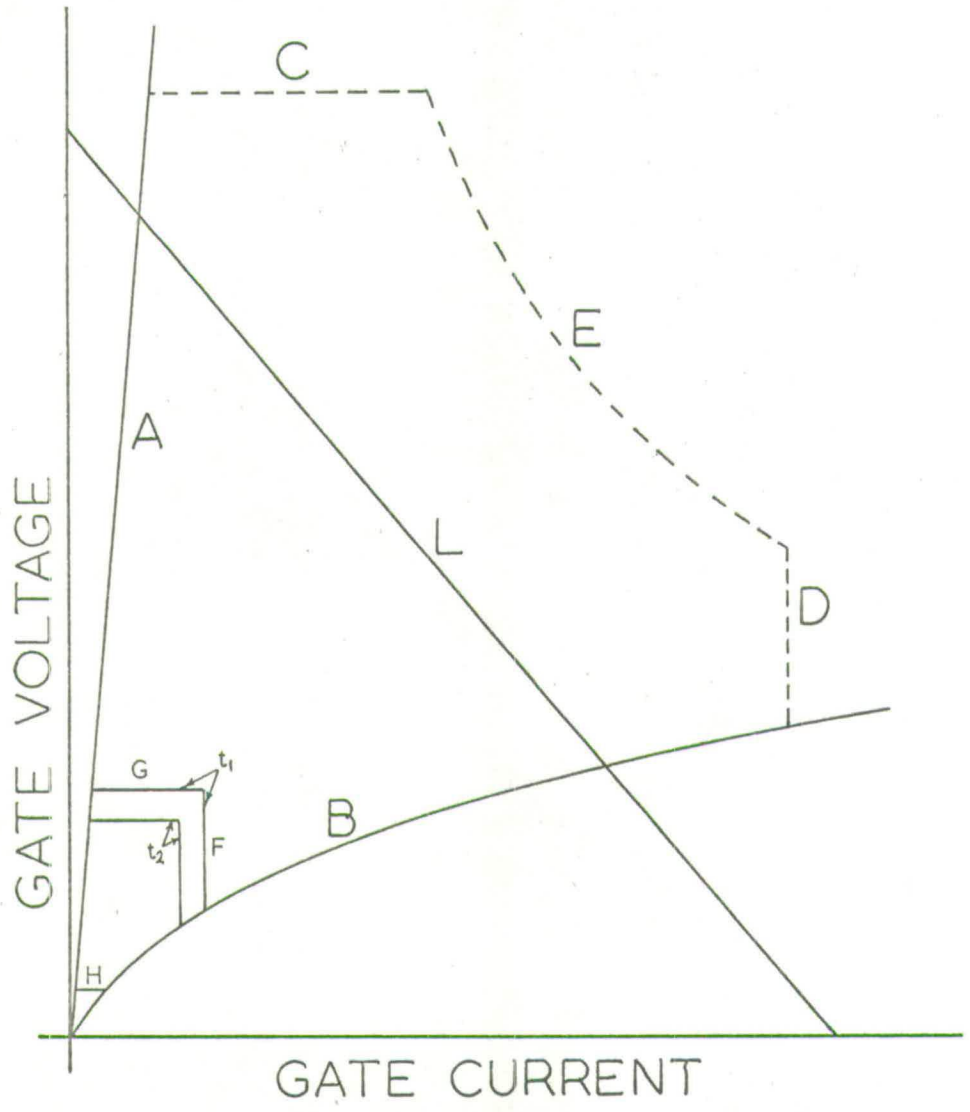
Negative gate bias increases forward breakover voltage and dv/dt withstand capability. Some thyristor ratings allow operation with the gate in the reverse avalanche region (Fig.1.2(b)).

1.2.2 Effects of Anode Circuit upon Gate Circuit

When a thyristor is conducting, its gate and cathode are almost at the same potential; during turn-off initiated by reverse anode voltage, the gate voltage is initially that of the gate-cathode junction until this recovers, when the gate voltage follows anode voltage until the main reverse-blocking junction recovers, when the gate characteristics become those of Fig.1.2(b).

1.2.3 D.C. Gate Triggering Specifications

The D.C. gate characteristics for a thyristor are presented in the form of a graph similar to Fig.1.2.3. This shows gate-to-cathode voltage for all thyristors of the specified type, with zero anode current.



1.2.3

All thyristors of the type specified will have gate input V-I characteristics between the lines A and B, and the maximum rated values of voltage, current and power are shown at C, D and E respectively.

The area bounded by lines A G F B H contains all the possible trigger points (I_{GT}, V_{GT}) of all thyristors conforming to the specification. Upper limits G and F may be given more than one value corresponding to different operating temperatures; increasing temperature increases the gate sensitivity of a thyristor.

The trigger circuit load line must intersect the thyristor gate characteristic in the region above (I_{GT}, V_{GT}) in order to fire the thyristor. This is ensured by the load line passing above the region containing (I_{GT}, V_{GT}).

Turn-on time is reduced by the use of large gate signals with short rise times, but these should not exceed the rated values of voltage, current and power.

Quiescent output of the gate signal source must be such that the load line passes below the region containing (I_{GT}, V_{GT}) which usually has a base-line of + $\frac{1}{4}$ V.

1.2.4 Pulse Triggering

On a short-time basis, thyristors may be considered to be charge-controlled, as are transistors. The minimum charge required to fire a thyristor is of the order of the D.C. trigger current (I_{GT}) multiplied by 20 μs. The current required to fire a thyristor within about 100μs. is almost equal to I_{GT}.

Increased gate power ratings are usually given for pulse triggering, depending on the duty cycle.

A negative pulse may be used to fire a thyristor, applied to the cathode in a suitable circuit.

1.2.5 Turn-on Interval Characteristics

Delay time, t_d is usually defined as the interval between the rapid rise of a trigger pulse and the thyristor anode voltage falling to 90% of its initial value. Rise time, t_r is the time taken for the anode voltage to fall from 90% to 10% of its initial value, as anode current rises. Total switching time $t_{on} = t_d + t_r$.

t_d decreases with increase of gate current, approaching a minimum for ordinary thyristors of 0.2 to 0.5μs.

Jitter, or variation of switching time from one cycle to the next, is usually less than 2 n.s.at constant temperature if the gate is driven at 2 to 3 times the minimum amplitude required for triggering.

1.3 Trigger Circuits

1.3.1 Resistor, Capacitor and Diode

Variable resistance connected from anode to gate of a thyristor may be used to give phase control by the increase of both gate current and gate sensitivity with increasing anode voltage. Firing angle is controlled on the anode voltage rising from zero to a maximum, over a 90 degree maximum range.

Phase control of an a.c. load may be given by the addition of a second thyristor in inverse parallel with the first; the

second thyristor is controlled by an R.C. integrating circuit which applies forward gate bias when the mean voltage across the thyristor becomes zero, integrated from the instant at which reverse bias first occurred on the thyristor anode.

Diodes may be used in both the above circuits to prevent application of reverse gate bias to the thyristors.

1.3.2 Thyratron Type

The gate of each thyristor is fed with a half sinusoidal current waveform, of large magnitude so that turn-on occurs at the beginning of each half-sinusoid; the delay mechanism may be an R.C. or R.L. circuit, usually fed at about 30 v.r.m.s. through a step-down transformer.

The low impedance of thyristor gate inputs necessitates the use of impedance to convert the voltage sinusoid into a gate current sinusoid; negative half cycles may be diverted or blocked by diodes.

1.3.3 Saturable Reactors

These components may be used as current-controlled timing elements, and may also initiate rapidly rising pulses by the abrupt change of inductance at saturation.

The simple timing circuits described in the previous sections depend on the specific triggering characteristic of the thyristor concerned; efficiency is usually low because current drawn by the trigger circuit from the high voltage supply is of the same order of magnitude as the trigger current.

1.3.4 Semiconductor Trigger-Pulse Generators

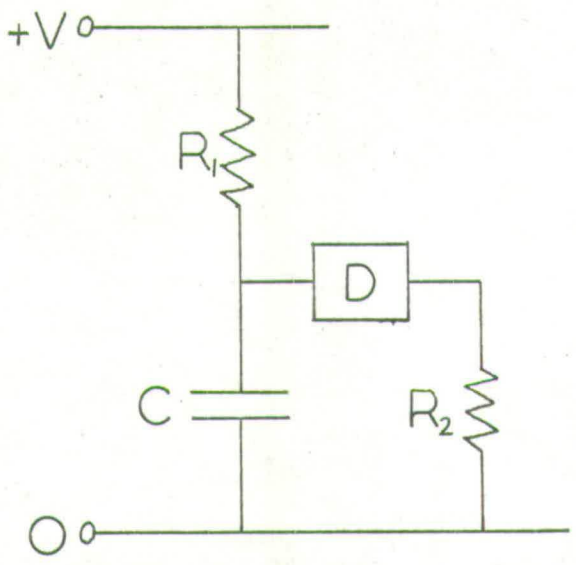
These can accommodate wide variation of trigger characteristics by overdriving the gate; mean power level is low since the pulses occupy only a small part of the total cycle time, and the circuits lend themselves readily to automatic, programmed or feedback control.

Devices specially suited to producing trigger pulses are:

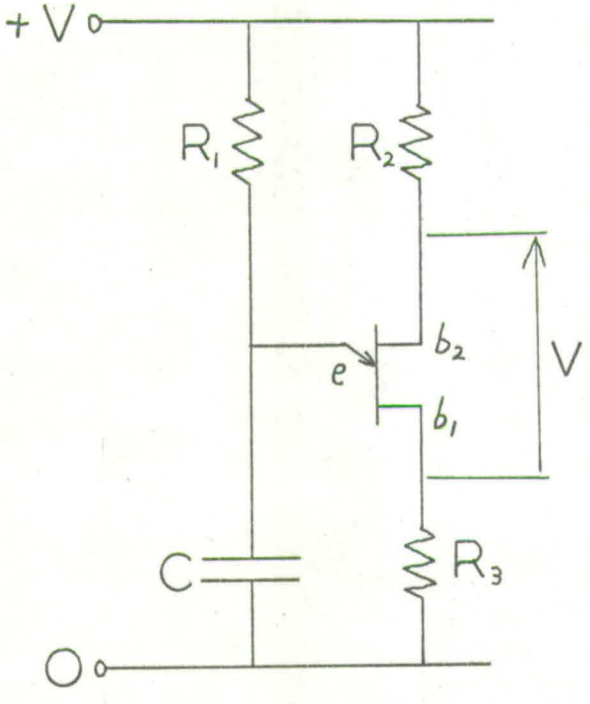
1. unijunction transistor
2. diac trigger diode
3. silicon unilateral switch
4. silicon bilateral switch
5. neon lamp

These devices and others have characteristics with negative-resistance regions and may be used to generate pulses in synchronism with an a.c. supply, or in relaxation oscillator circuits. In both these cases, charge stored over a large part of a cycle is released rapidly in a short pulse, minimising input power requirements and giving short thyristor turn-on time, with minimum dependence on the specific thyristor triggering characteristic.

Type 5 is a high voltage, low current device and thus suitable for firing only small thyristors, types 3 and 4 each contain thyristor-type p-n-p-n structures, type 2 is a 3-layer transistor having only 2 terminals. Types 1,3 and 4 each have 3 terminals, so that triggering can be initiated by more than one method. In type 1, the triggering point is reached at a certain ratio of 2 independently applied voltages; the absolute values of these may be chosen to suit the application.



1.3.4(a)



1.3.4(b)

The circuit of Fig.1.3.4 (a) illustrates the action of a relaxation oscillator using a 2-terminal trigger device D. Capacitor C is charged from the d.c. supply through resistor R_1. When capacitor voltage reaches the peak point voltage of the trigger device the latter turns-on, discharging the capacitor rapidly through R_2. In this case, R_2 may be replaced by a load such as a thyristor gate, or a more complex coupling may be used between pulse source and load.

Fig. 1.3.4 (b) shows a unijunction transistor relaxation oscillator; capacitor C is charged from the d.c. supply through R_1 as in the previous circuits. When the voltage between emitter (e) and base 1 (b_1) of the unijunction transistor reaches a certain fraction of the interbase voltage V_{bb} the device turns on, discharging the capacitor rapidly through load R_3.

Both the above oscillators may be synchronised by application of pulses to initiate the main output pulse before it would otherwise have been produced, or by charging the capacitor from a time-varying supply.

The circuit using the 3-terminal device offers more scope for synchronising methods as the pulse can be initiated by momentary reduction of interbase voltage.

The circuit in both cases must supply capacitor charging current which is sufficiently low to allow the trigger device to turn off at the end of each pulse.

Most semiconductor trigger devices have switching times in the region 0.5μs. to 5μs. Where the thyristor must conduct large initial di/dt, a gate pulse source using a high speed switching transistor is more suitable.

1.3.5 Thyristors as Gate Signal Amplifiers

A thyristor T_1 having low triggering current may be used to trigger a high current thyristor T_2 by connection as shown in Fig.1.3.5. The anode voltages applied to T_1 and T_2 are similar, but T_1 conducts only momentarily and cooling requirements will be negligible. This arrangement may be used to turn on thyristors connected in parallel with T_2, by use of resistors to force current sharing between the thyristor gates.

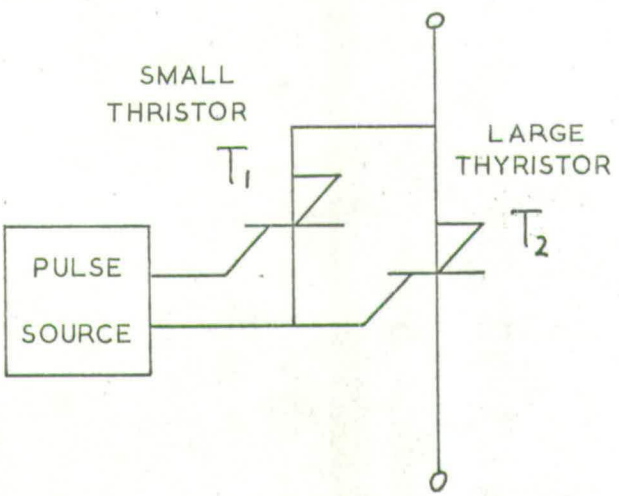
1.3.6 Pulse Isolation by Transformer

Leakage inductance should be low to minimise rise time of the output pulse, and capacitance between primary and secondary circuits should be low to minimise unwanted coupling. The voltage time integral of a thyristor firing pulse is small because of the low input impedance of the gate and the short duration of the pulse. A small number of turns wound on a small cross-section core will support the pulse voltage without giving rise to excessive magnetising current; bifilar or multifilar windings can thus be used to minimise leakage inductances without incurring large winding capacity.

Application of reverse gate bias to the thyristor during resetting of the transformer core may be prevented by suitable use of diodes, or minimised by limiting the resetting voltage.

1.3.7 Optical Pulse Isolation

Use of a carrier frequency in the region of 3×10^{14} c/s permits small devices to isolate signals with negligible unwanted coupling.


SMALL
THRISTOR
T_1
LARGE
THYRISTOR
T_2
PULSE
SOURCE

Light activated silicon semiconductor devices respond to radiation of 0.6 to 1.1 microns wavelength with maximum sensitivity in the region 0.9 to 1.0 microns. Sources of light with wavelengths in this region are:

1. tungsten lamps
2. light emitting diodes
3. xenon flashtubes

Neon lamps are not in this category. Type 1 has slow response caused by thermal inertia of the hot filament, type 2 has fast response, 20 ns. rise time and 200 ns. fall time, but is expensive; type 3 has fast response and produces a flash of great intensity, but requires a pulse of several kilovolts to trigger it.

Light may be used to trigger a thyristor directly or a light activated thyristor or silicon controlled switch or phototransistor may be used to provide amplification. The phototransistor has a progressive response to increase of light intensity, the other two are latching devices. Photofransistor circuits can react to very low light levels.

1.4 Inversion

Direct current power may be converted to a.c. power by the use of electronic valves through which conduction is controlled. The valves must have the ability to hold off forward voltage, and the time at which conduction starts to take place must be controllable.

Transfer of current from one valve to the next (commutation) involves reduction of forward current to zero in the first valve, delay of the reapplication of forward voltage to the valve until it has regained its forward blocking capability and buildup of forward current in a second valve.

In the simplest inverters, valves are used which can interrupt the current flow in response to an input signal; this change may be a gradual one so that load current is reduced slowly, or the change may be abrupt, in which case current in an inductive load must be given an alternative path.

Controlled electric valves of high power rating do not have the ability to interrupt load current in response to an input signal, and commutation in this case is one of the most difficult problems in inversion.

1.4.1 Thyristor Turn-off Methods

A mechanical switch in series or parallel with a thyristor will relieve the latter of load when operated and thus turn it off, but subsequent reversal of the switch setting results in reapplication of forward voltage to the thyristor at an uncontrolled rate; circuits have been devised to turn off or commutate thyristors satisfactorily without use of mechanical switches.

Reverse recovery current flows in a thyristor at the start of the turn-off period for a time known as the reverse recovery time, of order a few microseconds. Cessation of reverse recovery current can be abrupt, and can cause large voltage transients and radio frequency interference. In some inverter circuits, reverse recovery current of one thyristor is carried by another thyristor in the forward direction giving high initial di/dt in the latter.

1.4.2 Inverter Circuit Classification

Inverter circuits are classified by the method of thyristor turn-off as follows:

Class A self commutated by resonating the load.

Class B self commutated by an LC circuit.

Class C C or LC switched by another load-carrying thyristor.

Class D C or LC switched by an auxiliary thyristor.

Class E external pulse source for commutation.

Class F AC line commutated.

Class A inverters are most suitable for high frequency operation, because of the need for a resonant circuit to carry the full load current. In class B, if the load is in series with the thyristor, the LC circuit may be in parallel, so that coupling between LC circuit and load does not occur while the thyristor is conducting. Class C commutation is used when the load-carrying thyristors conduct alternately, as an a.c. coupling between them is all that is required; class D is used when forward voltage must be applied to a load-carrying thyristor before firing the next one in sequence, as in some inverters for motor control, and it may be used when there is only one load. It can take the form of a class C circuit with one of the loads a dummy. Class E includes application of a turn-off pulse by means not coming within classes A to D. In class F, the voltage reversals of an a.c. supply furnish negative anode voltage to turn a thyristor off.

1.4.3 Inverter Configuration

Chopper circuits and half-wave circuits apply pulses of d.c. to the load; centre taps may be used on the load or on the supply to eliminate the direct component, leaving only alternating voltage across the load. A centre tap may be provided for a

2-terminal laod by the use of a transformer; this may also give electrical isolation of the d.c. and a.c. circuits.

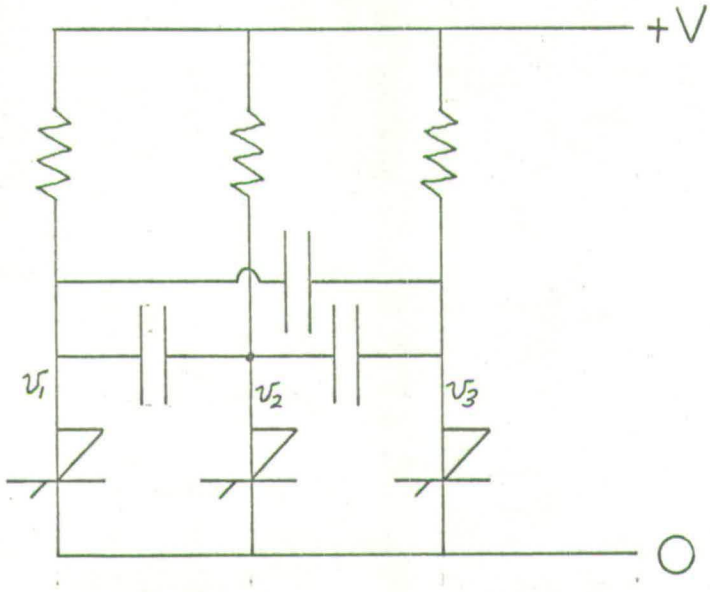
In bridge inverters, an increased number of thyristors are used to connect each load terminal to positive and negative sides of the supply in turn during each output cycle, thus dispensing with the need for centre taps.

The inverter used in the present work comprises two 3-phase bridge inverter groups coupled magnetically on the a.c. side, and fed from a common d.c. supply. Operation is explained in subsequent sections, starting with the half-wave ring-of-3 inverter.

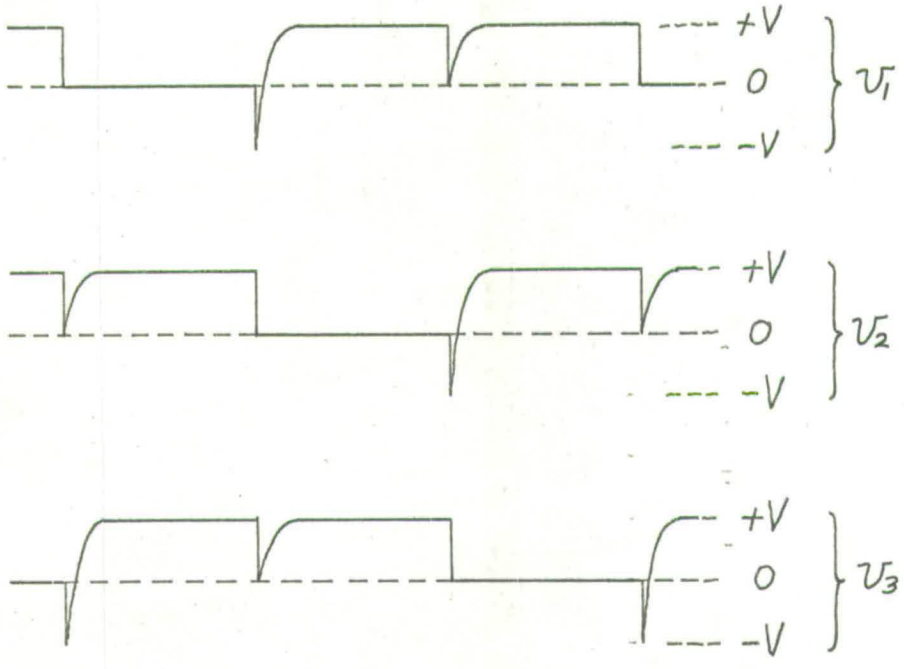
1.5 Ring-of-3 Inverter

This is illustrated in Fig.1.5(a) with class C commutation by capacitors C coupling the thyristor anodes. The thyristors are fired in rotation by application of gate pulses. The capacitors are charged to equilibrium through the resistors and thyristors between gate pulse applications, so that turn-on of each thyristor results in sudden application of reverse voltage to the previously conducting one, turning it off. Anode voltage waveforms, Fig.1.5(b) show the exponential decay of the commutating pulses, giving low-values of dv/dt which do not result in unwanted thyristor turn-on.

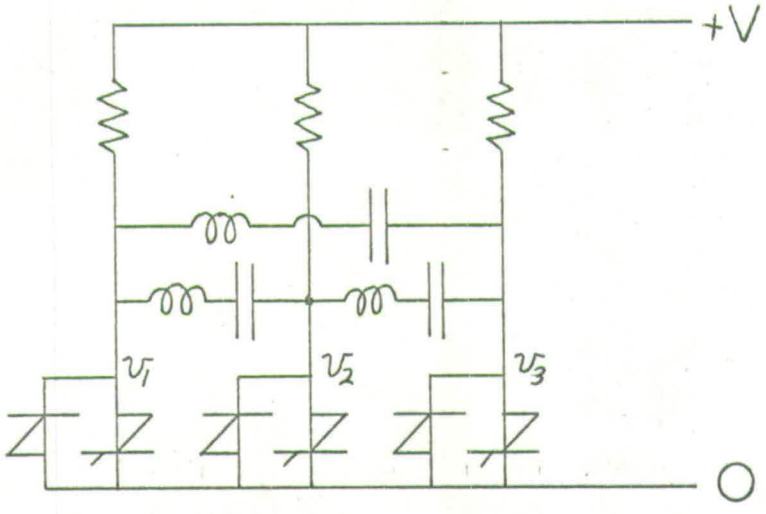
Commutation with limited reverse voltage is possible using the circuit of Fig.1.5(c); in this case, diodes limit reverse thyristor anode voltage and a series LC circuit forms the commutating coupling between thyristors. Application of a gate pulse to a



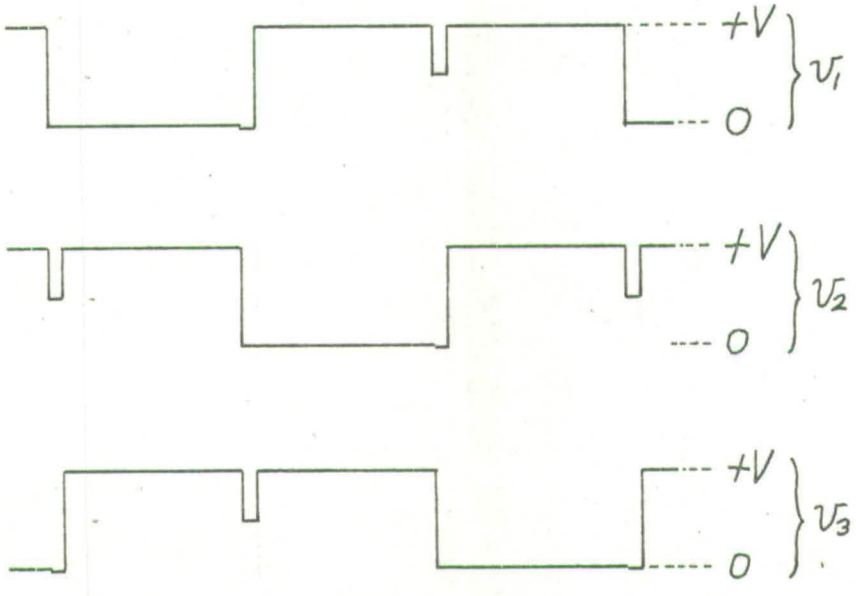
1.5(a)



1.5(b)



1.5(c)



1.5(d)

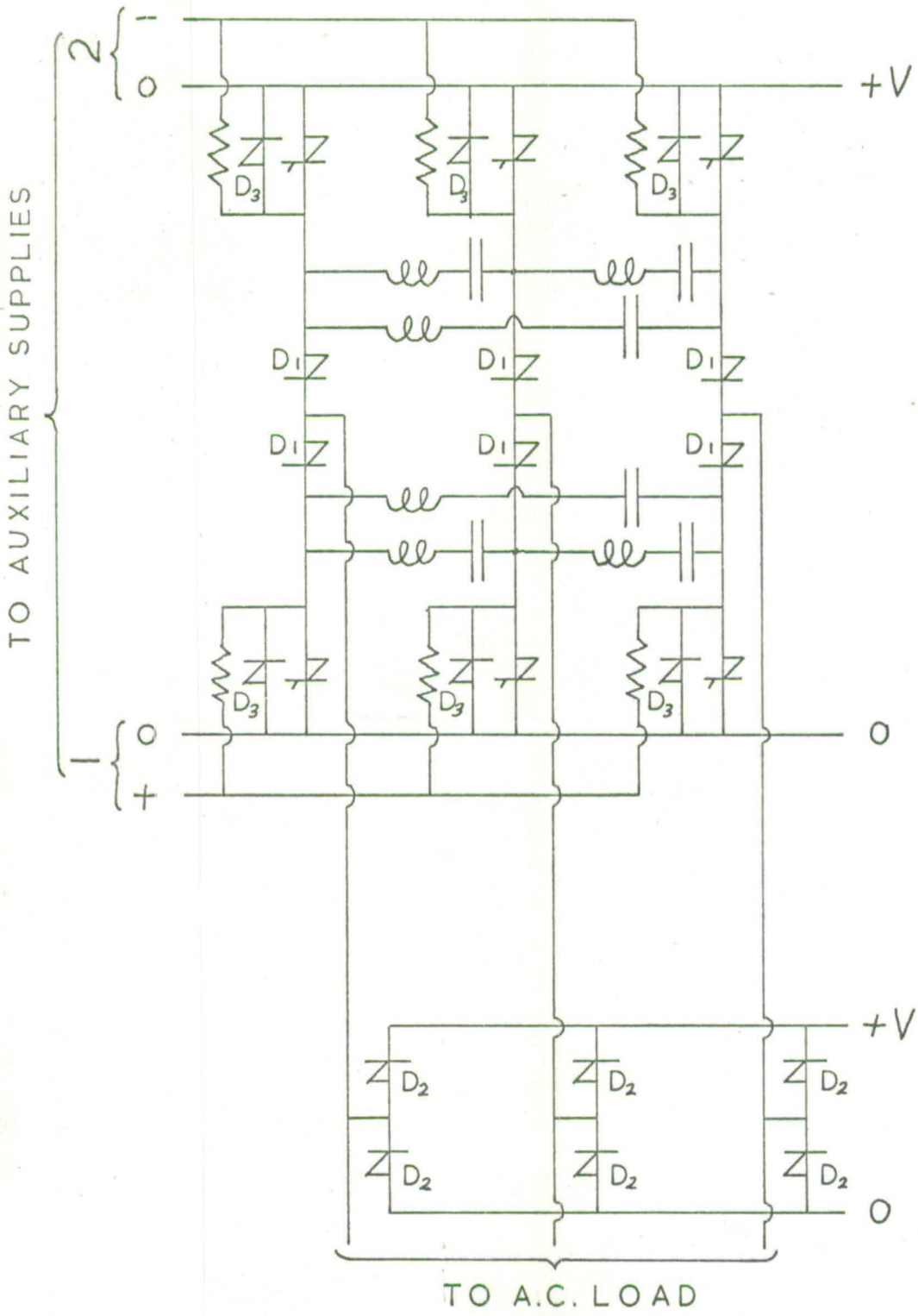
thyristor results in a half-sinusoid of current flowing through it and the LC circuit; the excess of this over load current in the previously conducting thyristor flows through a diode in inverse parallel with it, giving 0.7 volts reverse bias mementarily which turns off the thyristor. Most of the energy stored in the capacitors before the commutation is returned during the latter part of the oscillation; the effects of the commutating pulse on load voltage is minimised (for parallel commutation), Fig.1.5(d). A resistor and capacitor (not shown) are connected in series from anode to cathode of each thyristor to limit dv/dt.

1.5.1 Single 3-phase Bridge Inverter

Two ring-of-3 circuits are combined to form the bridge inverter, Fig.1.5.1. Diodes D_1 in conjunction with the auxiliary supplies render commutation currents independent of main supply voltage V_1 giving this wide useful range. Diodes D_2 allow power feedback from the a.c. circuit to the d.c. circuit at any part of the operating cycle so that reactive loads may be fed. Feedback may be either directly to the supply or via a balancing circuit, which is of particular importance in the double-3-phase inverter discussed below.

Economy can be effected by omission of diodes D_3. Diodes D_1 in series with D_2 perform the same duty of conducting excess commutating current round the LC circuit, via the balancing circuit if one is used, and provided the balancing circuit permits.

Table 1.5.1 relates inverter output voltages to the thyristor firing sequence; the feedback diodes are assumed to be coupled



1.5.1

CLOCK PERIOD	1	2	3	4	5	6	
THYRISTORS ON	1 6	1 2	3 2	3 4	5 4	5 6	
POTENTIAL AT A,B,C	≤V ≥O	≤V ≥O	≤V ≥O	≤V ≥O	≤V ≥O	≤V ≥O	RECTIFIER
" A	≥V	≥V		≤O	≤O		INVERTER
" B	≤O		≥V	≥V		≤O	
" C		≤O	≤O		≥V	≥V	
" A	V	V	≤V ≥O	O	O	≤V ≥O	RECTIFIER AND INVERTER
" B	O	≤V ≥O	V	V	≤V ≥O	O	
" C	≤V ≥O	O	O	≤V ≥O	V	V	

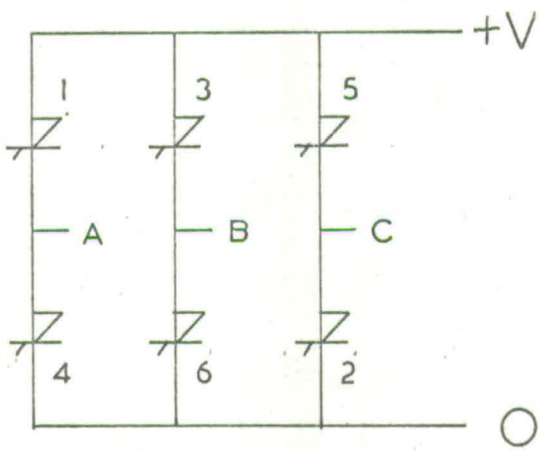


TABLE 1.5.1

directly to the d.c. supply, and clamping action of this is apparent. The periods in which output voltage is allowed some freedom are of especial use in parallel operation (next section) and in feeding machine windings.

1.5.2 Double 3-phase Bridge Inverter

Approximately sinusoidal output can be achieved by use of two 3-phase bridge inverters suitably coupled. Output phases are displaced an odd number of 30 degree intervals to give six phase operation. An interphase transformer may be used to couple the 3-phase inverters to the d.c. supply, or the feed to the thyristors and feedback diodes may be divided further by a balancing circuit.

This inverter operates with considerably lower ripple on the d.c. side and lower harmonic generation on the a.c. side and thus is more suitable for voltage control than the single 3-phase bridge circuit.

1.5.3 Thyristor Duty Cycles

During the conducting period of a thyristor, the anode current has components from several sources:

1. load
2. auxiliary supply
3. commutating circuit
4. dv/dt protection circuit

The load will usually have leakage inductance effectively in series so that instantaneous change of current is impossible. Load current may flow in either direction at any part of the cycle,

depending on load power factor. Also, power may flow at high frequency between coupled inverter groups and between inverter thyristor groups and feedback rectifiers; this represents thyristor load current and depends on the external load e.m.f.

Load current is carried by the thyristor when the direction of flow corresponds to forward thyristor current, hence the thyristor must be able to accommodate sudden build-up of load current at the start of the conduction period.

Rapid reversal of load current may result in momentary application of reverse bias to a thyristor during the reverse recovery time of an inverter diode.

Auxiliary supply current reaches each thyristor directly via resistors and indirectly as stored charge in the commutating circuit. The direct component ~~has a digital character; and~~ may be used as a holding current supply for the thyristor.

The commutating circuit supplies a pulse of forward current to each thyristor at the beginning of its conducting period. With simple capacitor commutation this is load current diverted from another thyristor, with abrupt rise and approximately exponential decay; with limited inverse voltage commutation the pulse has approximately half sinusoidal shape. The oscillation proceeds slightly beyond the current zero until the diode which carries excess commutating current has recovered reverse blocking capability.

When the main direct supply voltage approaches or exceeds auxiliary supply voltage, the commutating components are charged from the former source. Charging is impulsive because of

dependence on the inverter switching sequence, and may have slight resonances. Charging current flows through the thyristors, resonances may momentarily result in reverse bias of the thyristors.

The simple thyristor dv/dt limit circuit supplies a small current at turn-on; this decays exponentially with time constant of order 10 μs. This source may be used to supply latching current to the thyristor, if anode holding is used; the increased anode current at turn-on helps to hold the thyristor on if gate and holding currents are marginal.

Reverse blocking voltage need only be withstood by a thyristor during turn-off with simple capacitor commutation; peak value is equal in magnitude to peak forward voltage, and rate of decay depends on load current and auxiliary supply current.

Forward blocking voltage must be withstood by the thyristors in all normal inverters, in this case for 2/3 of each inversion cycle, less comutation time. Magnitude is ideally constant at auxiliary supply voltage or main supply voltage, whichever is the greater. In practice, commutations of other thyristors in the inverter superimpose pulses on this constant value, having considerable dv/dt in the case of the limited inverse voltage circuit.

1.5.4 Gate Signal Requirements

Gate current must be large at turn-on, with short rise time to minimise thyristor turn-on time. Firing pulses must have large amplitude until anode conduction is well established; if anode

current is available, conduction spreads over the whole junction area in about 10μs, thus firing pulse duration need not exceed this figure.

In the absence of a scheme to maintain anode current above the holding value against diode reverse recovery current and negative pulses from the commutating circuit, gate holding must be used. This gives freedom to design auxiliary supplies without reference to anode holding current, and inverter diodes need not have specially short recovery time.

Gate control in the thyristor blocking period is usually passive, i.e. no power is fed to the gate. With large thyristors and shorted emitter types, application of reverse gate current has little effect; with other types, this helps to maintain the blocking condition of the thyristor and reduces power loss caused by leakage current. Impedance connected from gate to cathode provides a path for controlled gate current, but also diverts current from the firing and holding pulse sources.

Capacitance connected from gate to cathode is not compatible with rapid gate voltage rise at turn-on; pure inductance similarly placed is not compatible with gate holding for long periods, e.g. at low inversion frequency. The effects caused by these impedances must be modified by additional circuitry if the firing and holding pulses are to reach the gate relatively undistorted. Gate-cathode resistance is specified by the makers for some thyristors; this usually has a value which is high compared with gate input resistance at triggering point, therefore does not attenuate gate signals unduly.

Intervals between successive inverter commutations must be equal except during system frequency or phase transients to minimise ripple on the d.c. side and harmonic generation on the a.c. side; this must follow from the application of firing pulses to the thyristors in sequence at exactly equal time intervals. Gate holding pulses must be maintained until initiation of the turn-off pulse, when the next thyristor in the same ring-of-3 is fired.

Gate signal sources are preferably isolated from each other and from any extensive circuitry to minimise coupling due to stray impedances. Control circuits are particularly vulnerable to pick-up caused by the virtually instantaneous voltage and current changes produced in the inversion process.

1.5.5 Solution Adopted

Equal time intervals between successive firing pulses are assured by the use of a single "clock pulse" source to initiate all firing pulses, distribution is by ring counter. Firing pulse duration is controlled by the output from a separate timer, adjustable from zero to 40μs; each holding pulse is initiated by the start of one firing pulse and terminated by the start of the firing pulse for another thyristor in the same ring-of-3.

All output pulses are produced by high speed switching transistors; isolation is by transformer, giving adequate isolation together with high transmission efficiency so that pulse forming or amplification need not be used after the isolation stage. Droop is given by use of resistors; these are placed in the primary

circuit of each transformer to minimise transformer voltage-time integral and to limit damage arising from malfunction of the circuit, for example while the circuit is being tested.

The question of holding pulse voltage-time integral and its dependence on output frequency has been overcome by use of a high frequency carrier system; a square a.c. waveform is used to minimise switching losses and to minimise carrier frequency harmonics fed to the load.

Design is simplified by the use of standard components; similar transistors are used for all functions, and output pulse o/c. voltage and s/c. current are determined by the d.c. supply voltage and transistor current ratings respectively. Output can be increased to meet specific requirements by use of higher rated components, or reduced by attenuation.

Clock pulse generator output frequency is proportional to a direct control current, therefore automatic frequency control may be easily applied. For synchronous operation, a phaselock loop is used in which the output from a phase comparator controls clock pulse frequency ($d\phi/dt$). Phase is controlled by the introduction of a direct current into the loop between phase comparator and clock pulse generator; variation of control current changes $d\phi/dt$, until ultimately balance is restored with a new value of ϕ.

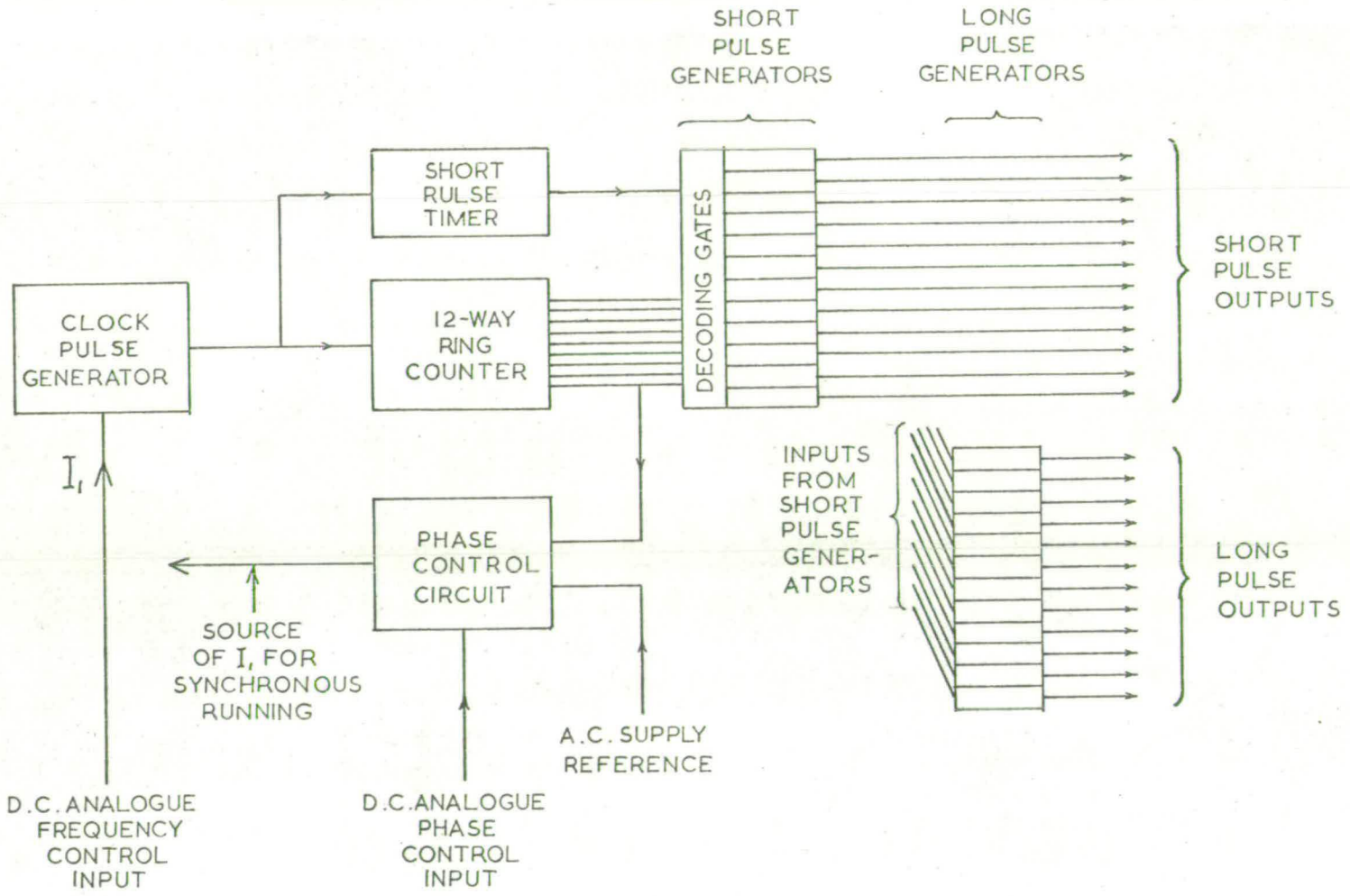
CHAPTER 2

THE PULSE GENERATOR

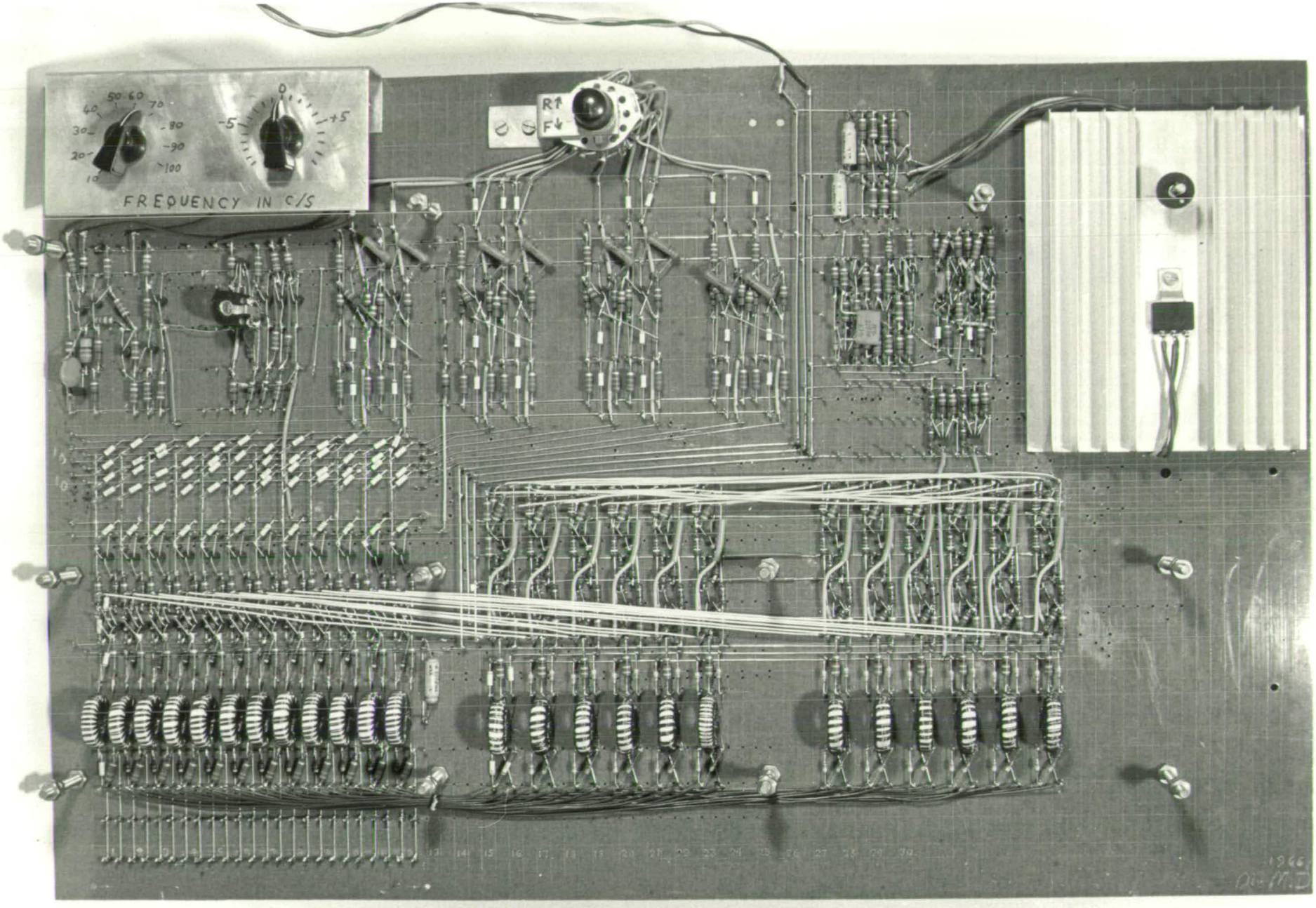
Fig. 2.1(a). A variable-frequency clock-pulse generator drives a ring-counter and a timer. These in turn control 12 short-pulse generators which produce pulses at isolated outputs in sequence as directed by the ring counter. Initiation of an output pulse occurs at the end of a clock pulse; the duration of the output pulse is controlled by the pulse timer.

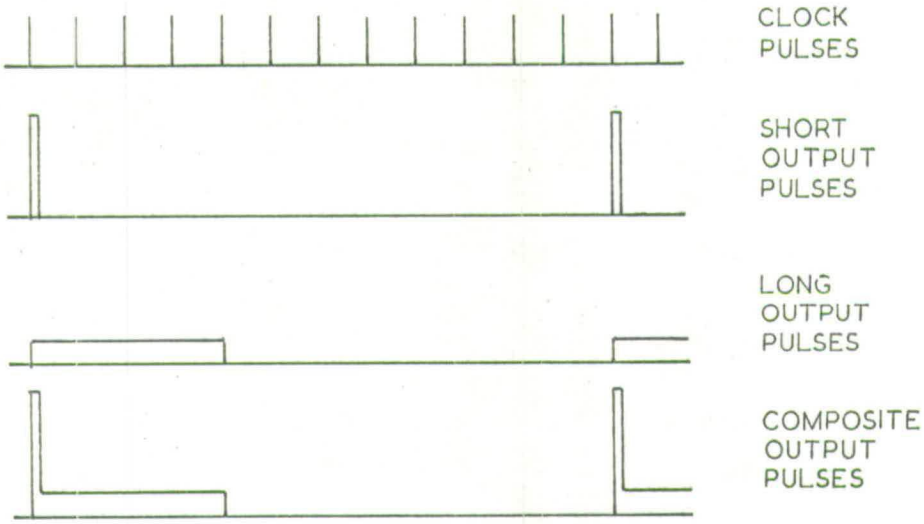
The ring counter output is in coded binary form, with an AND gate in each short-pulse generator to recognise the particular combination for which that pulse generator must produce a pulse. An additional input on each AND gate is fed from the pulse timer, to restrict the production of output pulses to the appropriate part of each clock period.

Twelve long-pulse generators produce rectangular pulses each of duration four clock periods. A high-frequency carrier coupling permits the long-pulse outputs to be isolated without restriction of the long-pulse duration. Additionally, each long pulse generator incorporates a bistable circuit, so that the control signal fed to it need not be continuous. The turn-on signal for each long-pulse generator is derived from the corresponding short-pulse generator, to start the short and long-pulses simultaneously. Pulses from both short and long-pulse generators are applied in parallel to a thyristor gate to turn on and to hold on the thyristor. The composite pulse Fig. 2.1(b). is particularly suited to gate control of thyristors.


SHORT PULSE GENERATORS
LONG PULSE GENERATORS
SHORT RULSE TIMER
DECODING GATES
SHORT PULSE OUTPUTS
CLOCK PULSE GENERATOR
12-WAY RING COUNTER
INPUTS FROM SHORT PULSE GENER-ATORS
LONG PULSE OUTPUTS
I_1
PHASE CONTROL CIRCUIT
SOURCE OF I, FOR SYNCHRONOUS RUNNING
A.C. SUPPLY REFERENCE
D.C. ANALOGUE FREQUENCY CONTROL INPUT
D.C. ANALOGUE PHASE CONTROL INPUT

2.1(a)


40
50
60
70
30
80
20
90
100
10
FREQUENCY IN C/S
0
-5
+5
R↑
F↓

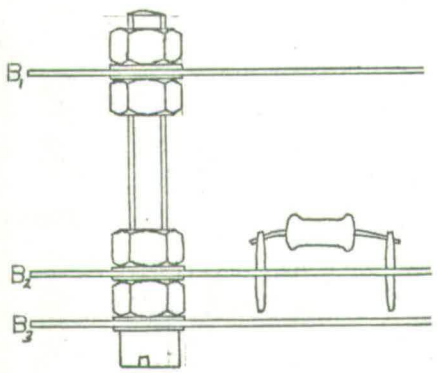


2.1(b)

B_1, B_2, B_3 – $\frac{1}{16}$" THICK S.R.B.F.

SCREW – 2 B.A. x 2"

PINS – VERO 2140/3073



2.1.1(b)

Backward and forward sequence running are provided by arranging for a particular long-pulse generator to be turned-off by one or other of the short-pulse generators which are sequentially 4 steps behind or 4 steps forward of the initiating short-pulse generator.

Control of output frequency is by d.c. analogue signal which may be generated by potentiometer for open-loop control or a tachometer for automatic control.

The pulse generator may be synchronised to an a.c. supply and run with a controlled phase relationship to the supply. Alternating current reference signals from both the pulse generator and the a.c. supply, and a d.c. analogue phase control signal are fed into a phase control circuit. The phase control circuit feeds a control signal to the clock pulse generator, so that the difference in phase between the pulse generator output and the a.c. supply is a linear function of the d.c. analogue control signal. The complete circuit diagram is [illegible] back cover.

2.1.1 Construction

Fig. 2.1.1(a) is a general view of the pulse generator with cover removed, and Fig.2.1.1.(b) shows the method of construction. Circuit components were mounted on an insulating board B_2; boards B_1 and B_3 were used to provide additional mechanical strength, and an insulating outer cover. Board B_3 was made easily detachable for access to the circuit; all circuit components were mounted between boards B_2 and B_3, for ease of access.

2.1.2 The Power Supply

A 12-V d.c. stabilised source provides the basic supply;

intermediate potentials are derived by the circuit of Fig.2.1.2. An output at mid-potential from terminal B is derived by comparing the potentials of A and B ($R_1 = R_2$) and the amplification of the four transistors makes the voltage difference between terminals A and B virtually zero.

Potentials within the pulse generator circuits are usually referred to the supply mid potential. A further line is fed at $-1\frac{1}{2}V$ using the forward voltage drop across two silicon-junction diodes.

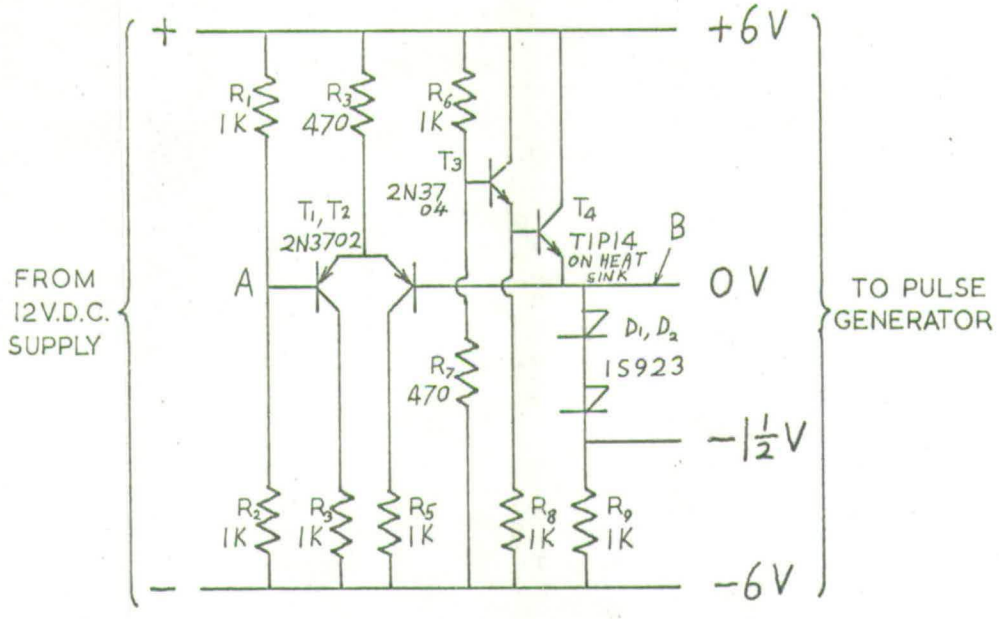
2.2 The Clock Pulse Generator

The circuit is shown in Fig.2.2.(a). The d.c. control current is fed through a buffer stage T_1 to charge capacitor C. A Schmitt trigger circuit (T_4 and T_5) has its input connected across the capacitor. When the capacitor voltage v_c reaches the upper hysteresis limit V_u of the trigger, transistor T_2 is turned on, to discharge the capacitor very rapidly. When v_c falls to the lower hysteresis limit V_L of the trigger, T_2 is turned off and v_c rises again under the influence of the control current.

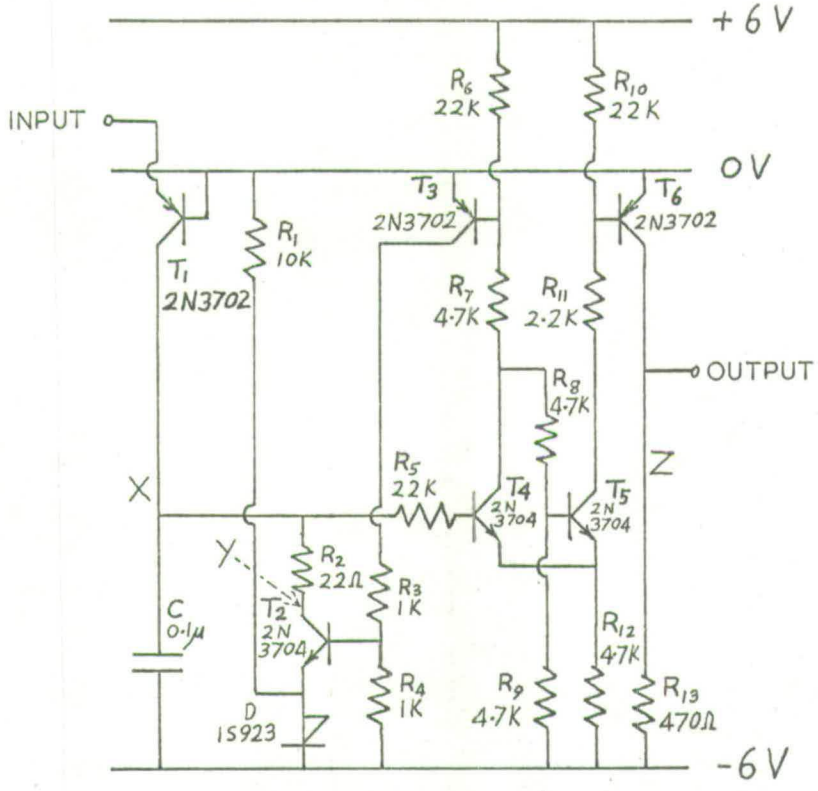
T_3 and T_6 are driven directly by the trigger; T_3 controls the base current to T_2, and T_6 is an output buffer.

During capacitor charge the output terminal is held at zero potential by T_6, and the output is taken as "dormant"; during capacitor discharge, the output terminal is negative and this forms a clock pulse.

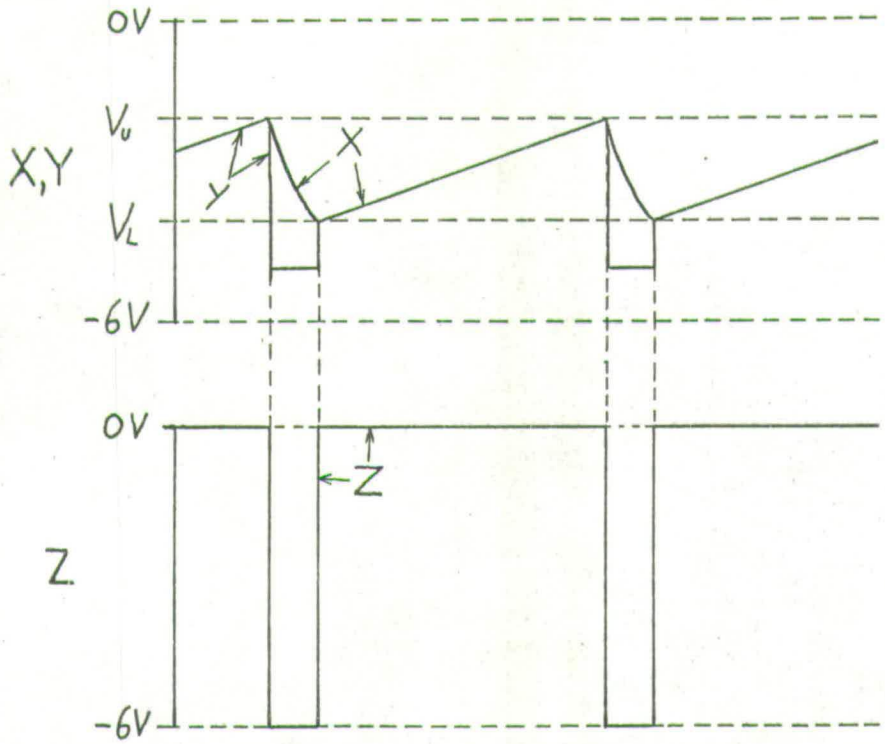
Fig. 2.2(b) shows idealized voltage waveforms at points X, Y and Z in Fig. 2.2(a); Fig.2.2(c) is an oscillogram of the same showing


+
−
+6V
0V
−1½V
−6V
FROM 12V.D.C. SUPPLY
TO PULSE GENERATOR
R1 1K
R3 470
R6 1K
T3 2N3704
T4 TIP14 ON HEAT SINK
T1, T2 2N3702
A
B
D1, D2 IS923
R7 470
R2 1K
R3 1K
R5 1K
R8 1K
R9 1K

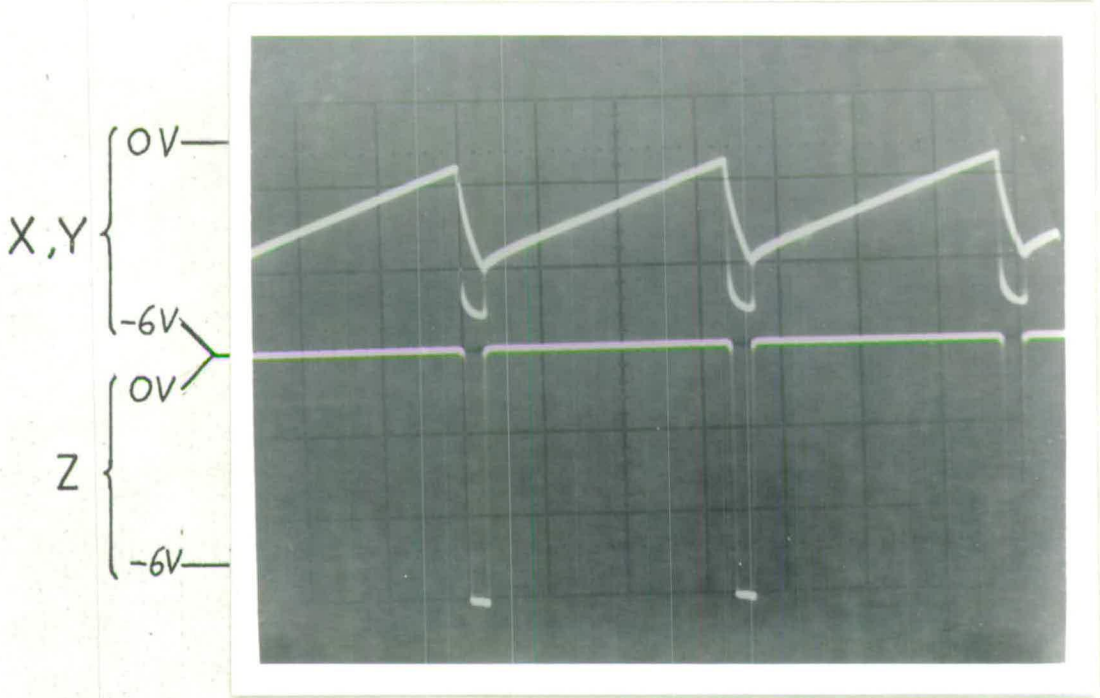
2.1.2


+6V
0V
−6V
INPUT
OUTPUT
R6 22K
R10 22K
T3 2N3702
T6 2N3702
T1 2N3702
R1 10K
R7 4·7K
R11 2·2K
R8 4·7K
X
Z
R5 22K
T4 2N 3704
T5 2N 3704
Y
R2 22Ω
R3 1K
C 0·1μ
T2 2N 3704
R12 4·7K
R4 1K
R9 4·7K
R13 470Ω
D IS923

2.2.(a)



2.2(b)



2.2(c)

slight divergence from the drawing caused by impedances not considered in the idealized operation.

The control characteristic is ideally of the form

$$f = AI$$

where f = the clock pulse repetition rate

A = the pulse generator constant

I = control current

2.3 The Ring Counter

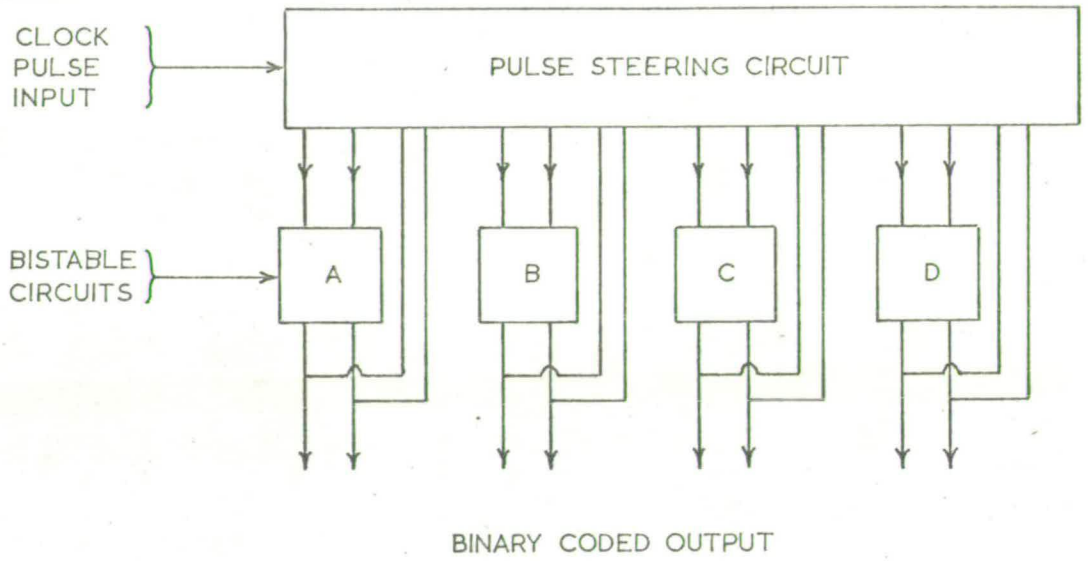
A binary coded system is used, in which each of the twelve states of the ring counter is represented by a particular combination of states of four bistable circuits. Fig. 2.3(a) is a block diagram of the system.

Clock pulses switch the bistables from one state into another, guided by a pulse steering circuit which distributes the pulses selectively. The pulse steering circuit is driven by the outputs from the bistables, and comprises delay circuits and diode gates. The complete circuit of the ring counter is given in Fig.2.3(b).

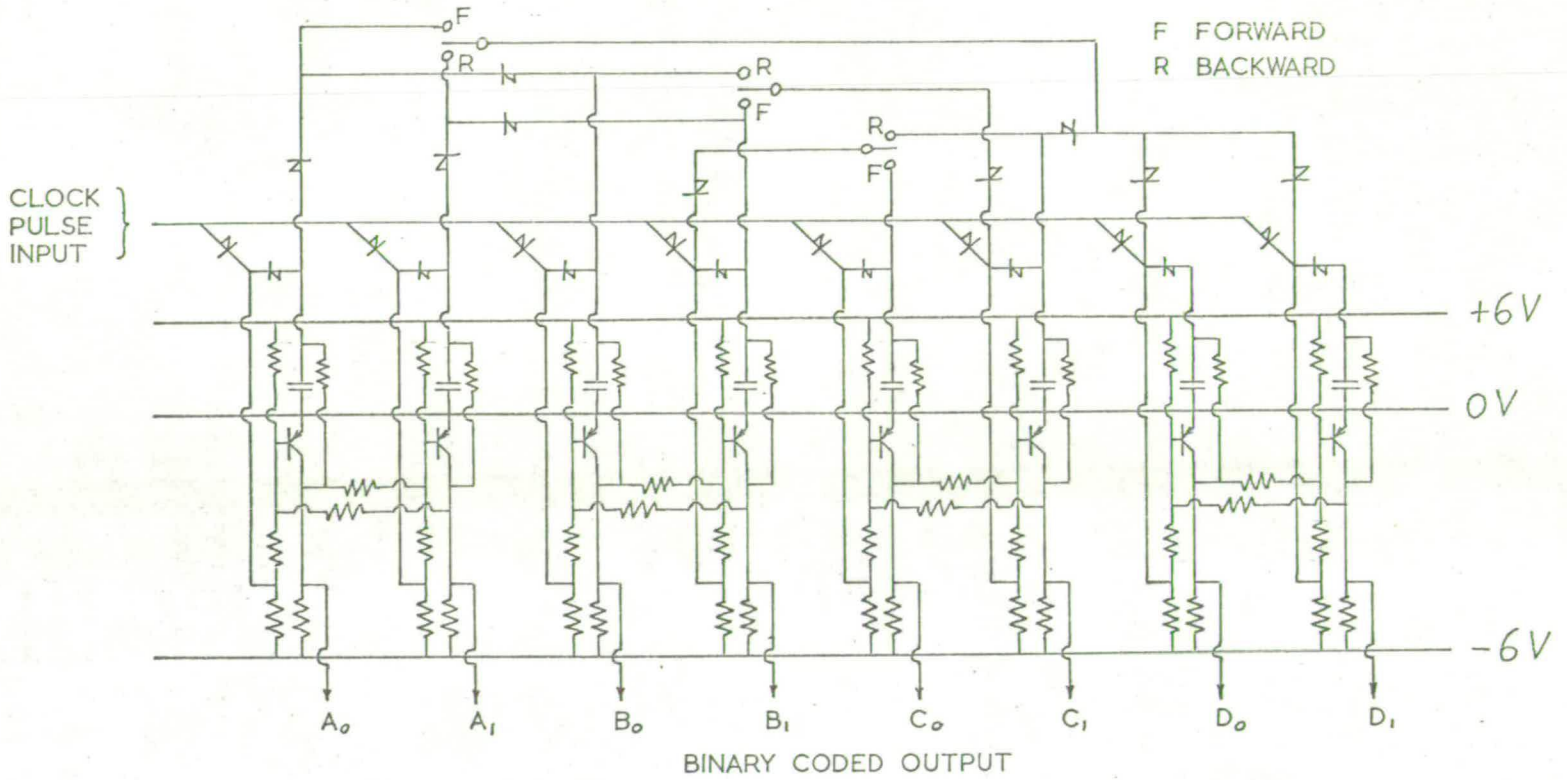
2.3.1 Bistable Circuits

Each bistable circuit has two PNP transistors as shown in Fig. 2.3.1.

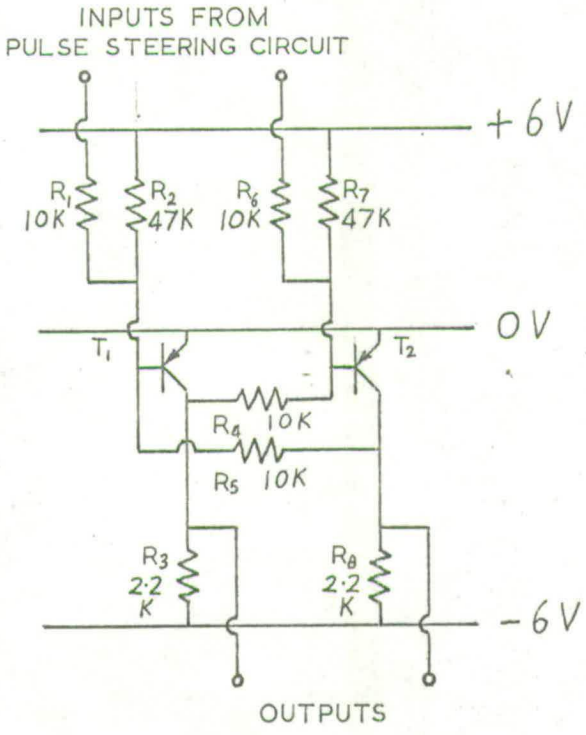
The base of each transistor is connected through a resistor to an input terminal, so that the application of negative going clock pulses changes the state of the bistable. The input terminal must be held sufficiently negative to exceed the margin of 6 R_1/R_2V. to apply forward bias to the base-emitter junction of the transistor;


CLOCK
PULSE
INPUT
PULSE STEERING CIRCUIT
BISTABLE
CIRCUITS
A
B
C
D
BINARY CODED OUTPUT

2.3(a)


F FORWARD
R BACKWARD
CLOCK PULSE INPUT
+6V
0V
-6V
A0
A1
B0
B1
C0
C1
D0
D1
BINARY CODED OUTPUT

2.3(b)


INPUTS FROM
PULSE STEERING CIRCUIT
+6V
R1
10K
R2
47K
R6
10K
R7
47K
0V
T1
T2
R4 10K
R5 10K
R3
2·2
K
R8
2·2
K
-6V
OUTPUTS

2.3.1

this allows slight variation in input voltage during suppressed clock pulses, and thus a simple pulse steering technique may be employed.

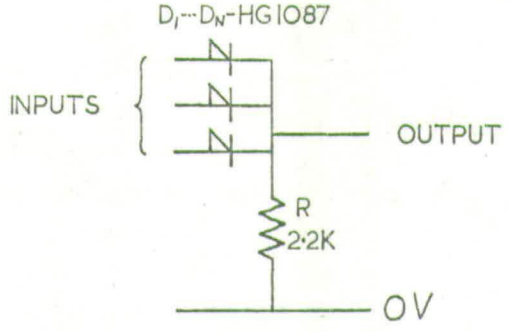
The output from the bistable circuit is taken from the collector terminals of the transistors, and can supply loads in parallel with R_3 and R_8 respectively across the 6-V supply. Two inputs and two outputs facilitate diode logic at input and output.

2.3.2 Pulse Steering Method

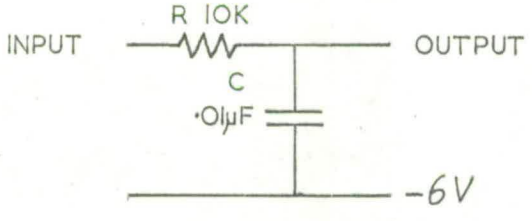
8 AND gates, Fig.2.3.2.(a) control the input to the bistables, and are fed with clock pulses and with some of the outputs from the bistables, via delay circuits, Fig. 2.3.2.(b)

In the absence of a clock pulse, the clock pulse generator holds one input terminal of each AND gate at zero volts, thereby holding the gate output and bistable input at zero volts. This has no effect on the bistable, and relieves the delay circuits of load, these then charge towards equilibrium.

During a clock pulse, the output of the clock pulse generator becomes negative allowing the outputs from the AND gates to be determined solely by other inputs from the delay circuits. The AND gate with negative inputs gives negative output and turns on the transistor of the bistable to which it is connected. If any input is at zero volts the output will be prevented from being sufficiently negative to change the state of a bistable. The delay circuits can supply sufficient charge to exert this inhibiting action for the duration of a clock pulse.


D1---DN-HG1087
INPUTS
OUTPUT
R
2·2K
0V

2.3.2(a)


R 10K
INPUT
OUTPUT
C
·01μF
-6V

2.3.2(b)

2.3.3 The Pulse Steering Circuit

A small number of interconnections between the ring counter elements makes the four bistables switch through twelve different combinations of states in sequence. Part of the pulse steering system is shown in Fig.2.3.3; the delay circuits are shown by boxes. All the diodes shown form the AND gates.

The gates controlling bistable D are compounded to use less diodes than would otherwise have been required. The three-pole, two-way switch is incorporated to reverse the output sequence. Diodes "R" prevent clock pulses from reaching both sides of a bistable simultaneously, and the other diodes further inhibit switching according to the laws shown in table 2.3.3.(a).

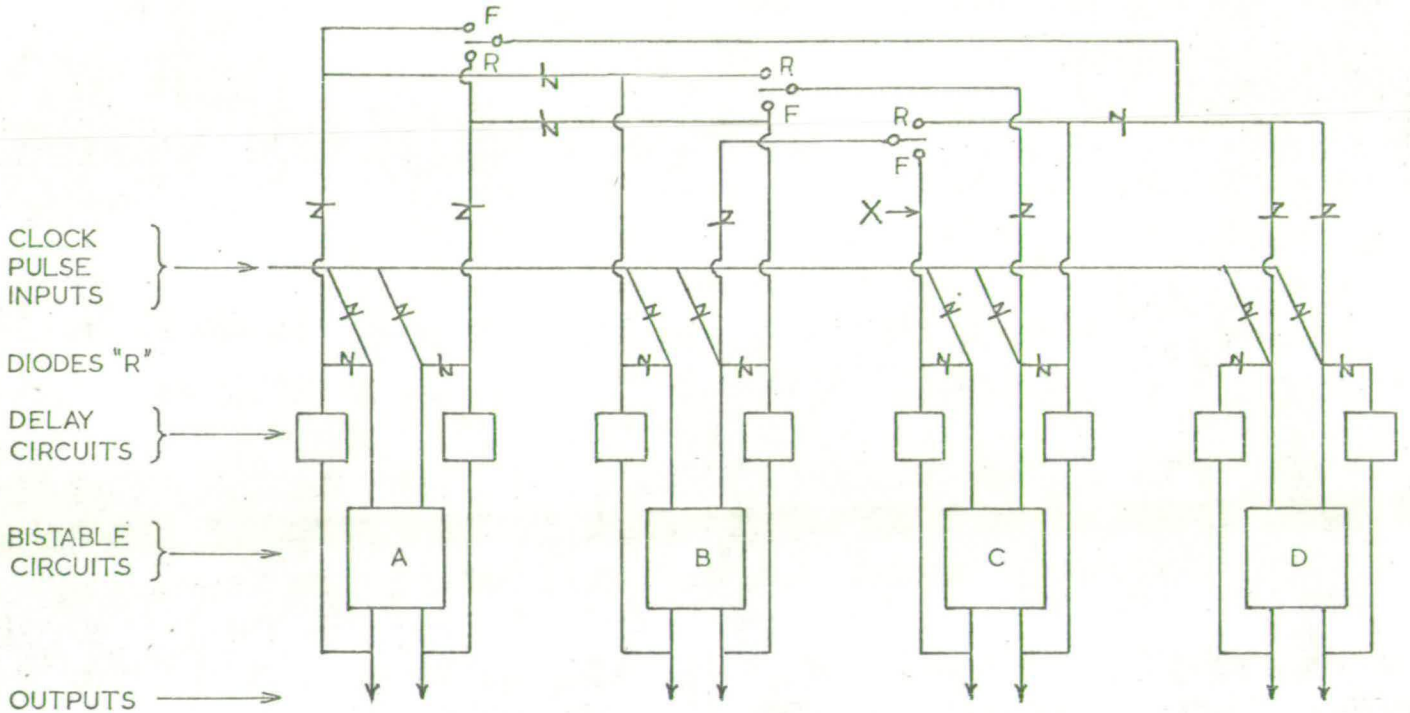
The notation is illustrated by the following example: "C_o inhibits B_1" in the "forward" column means that with the reversing switch in the "forward" position, and bistable C in state O, the next clock pulse cannot switch bistable B into state 1. The connection in Fig.2.3.2 marked X provides this effect.

Table 2.3.3(b) shows the output rota followed by the ring counter in response to the laws of table 2.3.3.(a). When the counter starts in one of the four possible states which are not in the rota, the first clock pulse will switch the counter into the rota.

2.4 Short Pulse Generation

2.4.1 Short Pulse Timer

In Fig.2.4.1. transistor T_1 inverts the incoming clock pulses, and holds the output voltage at zero during each clock pulse. Capacitor C discharges through T_1 during the clock pulse. After each clock pulse C charges slowly to a certain voltage at which the

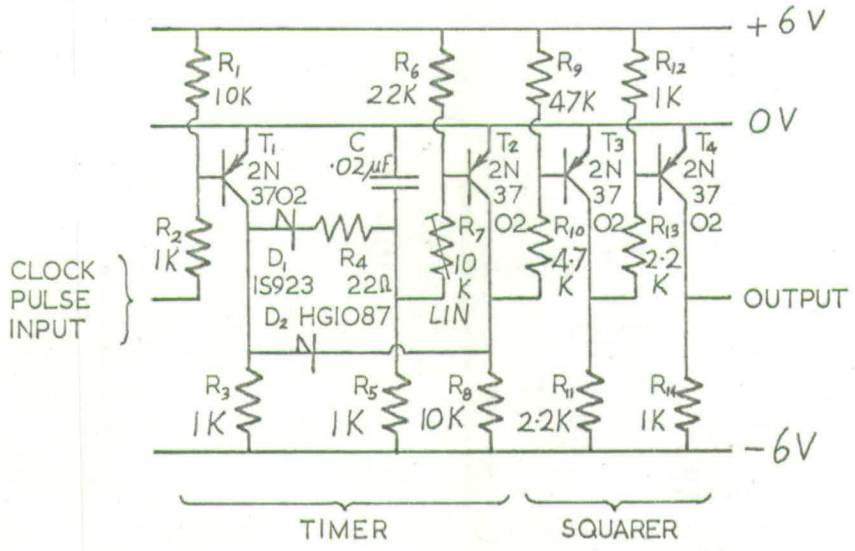

F
R
R
F
R
F
X
CLOCK PULSE INPUTS
DIODES "R"
DELAY CIRCUITS
BISTABLE CIRCUITS
OUTPUTS
A
B
C
D

FORWARD			BACKWARD		
C_0	INHIBITS	B_1	C_1	INHIBITS	B_1
B_1	"	C_1	B_0	"	C_1
A_0	"	D_0	A_1	"	D_0
B_0	"	D_0	B_1	"	D_0
C_1	"	D_0	C_1	"	D_0
A_0	"	D_1	A_1	"	D_1
B_0	"	D_1	B_1	"	D_1
C_1	"	D_1	C_1	"	D_1

2.3.3(a)

STATE OF RING COUNTER	1	2	3	4	5	6	7	8	9	10	11	12
" " BISTABLE A	0	1	0	1	0	1	0	1	0	1	0	1
" " " B	0	0	1	0	0	1	0	0	1	0	0	1
" " " C	0	1	0	0	1	0	0	1	0	0	1	0
" " " D	0	0	0	0	0	0	1	1	1	1	1	1

2.3.3(b)


+6V
0V
-6V
R1 10K
R6 22K
R9 47K
R12 1K
T1 2N 3702
C .02μf
T2 2N 37 02
T3 2N 37 02
T4 2N 37 02
R2 1K
D1 IS923
R4 22Ω
D2 HG1087
R7 10 K LIN
R10 4·7 K
R13 2·2 K
CLOCK PULSE INPUT
OUTPUT
R3 1K
R5 1K
R8 10K
R11 2·2K
R14 1K
TIMER
SQUARER

network applies forward bias to the base-emitter junction of T_2 so turning it on and holding the timer output at zero until the next clock pulse causes T_1 to discharge the capacitor again.

Diodes D_1 and D_2 isolate C from the timer output except when T_1 short circuits both of these and the zero potential supply line. An adjustable element R_6 couples C to T_2 to vary the duration of the negative output pulse. Transistors T_3 and T_4 square the output from the timer.

2.4.2 Short Pulse Generators

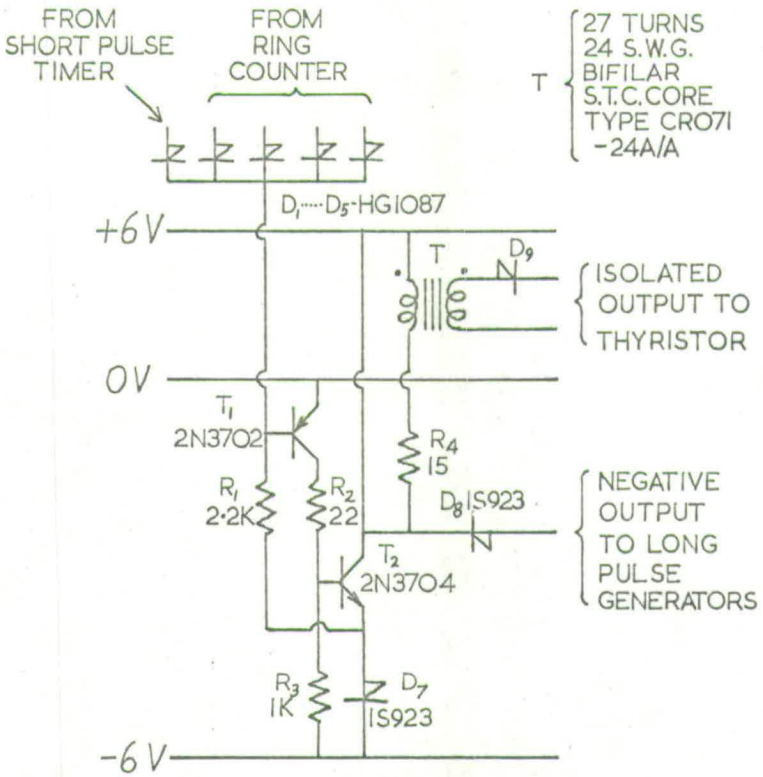
Twelve of these units are used, each has the circuit shown in Fig.2.4.2. Diodes D_1 to D_5 form a 5- input AND gate, with an output which is negative during a coincidence of the following:

(1) ring counter output in a given state

(2) short pulse timer output negative.

The gate responds to only one of the 16 possible ring counter output combinations by connecting one of the output terminals on each of the ring counter bistable circuits to an input of the gate. Thus, a short pulse generator with its AND gate fed from terminals A_o B_o C_1 and D_o of the ring counter, referred to in Fig.2.3(a) or (b) or Fig.2.3,3., responds only to state A_o B_o C_1 D_o of the ring counter. The remaining gate input terminal is connected to the short pulse timer output, so that the duration of the short pulse may be controlled by the timer.

When the gate output is negative, current carried by the gate load resistor R_1 is transferred to the base of transistor T_1, turning it on. T_2 provides further amplification and switches the output terminals across the 12V supply. Transformer T provides electrical isolation of the output, R_4 provides a resistive output characteristic


FROM SHORT PULSE TIMER
FROM RING COUNTER
T
27 TURNS
24 S.W.G.
BIFILAR
S.T.C. CORE
TYPE CRO71
-24A/A
D1 ···· D5 - HG1087
+6V
T
D9
ISOLATED
OUTPUT TO
THYRISTOR
0V
T1
2N3702
R4
15
R1
2·2K
R2
22
D8 IS923
NEGATIVE
OUTPUT
TO LONG
PULSE
GENERATORS
T2
2N3704
R3
1K
D7
IS923
-6V

and D_6 and R_4 accommodate the accumulated magnetizing current when the transistors are switched off, so protecting transistor T_2 from this duty.

Negative control signals are fed to the long-pulse generators through diode D_8. Diode D_9 prevents the transformer core resetting voltage reaching the load.

Diode D_7 and the -1.5V supply apply reverse voltage to the base-emitter junctions of T_2 and T_1 respectively when the transistors are turned off, to give a noise margin to the unit. The coupling between transistors T_1 and T_2 is a suitable point at which to add a speed-up capacitor if necessary.

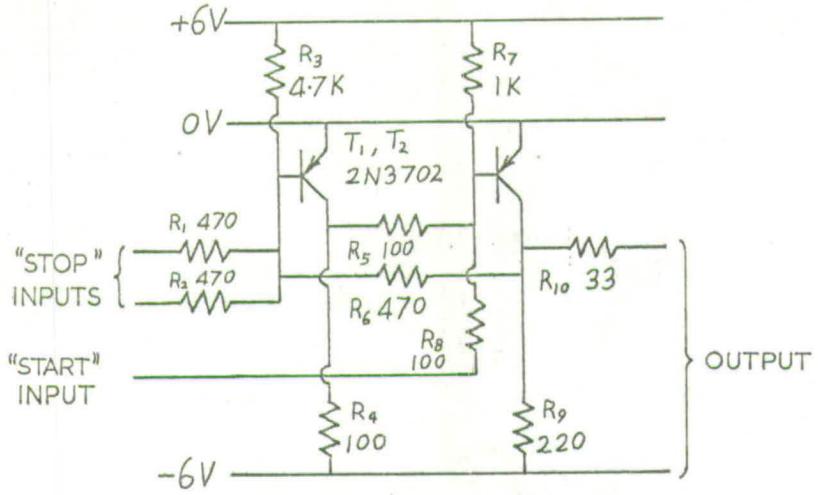
2.5 Long-Pulse Generation

2.5.1 Generation and Control

This was performed by 12 identical circuits, one of which is shown in Fig.2.5.1.

PNP transistors T_1 and T_2 are in a bistable circuit; the output is in parallel with the permanent collector load R_9 of T_2. The bases of T_1 and T_2 are connected through resistors to input terminals, so that the application of negative-voltage pulses may control the state of the bistable circuit. The output voltage is the supply voltage when T_2 is on, and a much lower voltage when T_2 is off. A single "start" input and two "stop" inputs are provided, to receive negative-voltage pulses from appropriate short pulse generators.

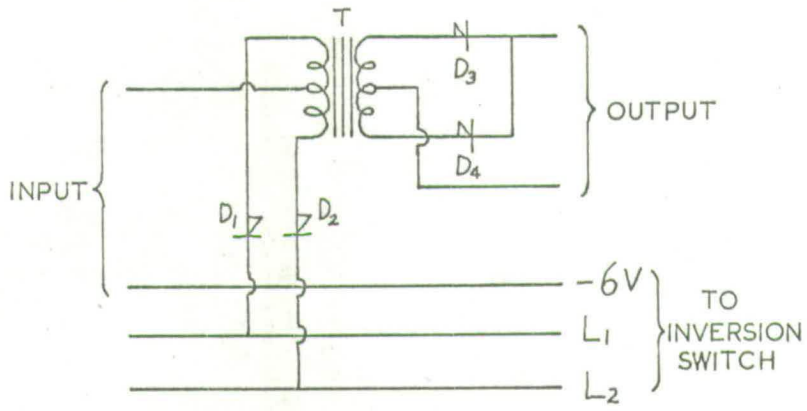
R_{10} provides the required output impedance. The small output voltage produced between pulses is almost completely suppressed in the isolation process, described in section 2.5.2.



2.5.1

D1 ··· D4 - 1S923

T - { 21 TURNS
28 S.W.G.
4 - FILAR
S.T.C. CORE
TYPE CRO71
-24 A/A



2.5.2

2.5.2 Isolation

In Fig.2.5.2 the input voltage is applied between the -6V line and the centre-tap on the transformer primary; the outer ends of this winding are alternately connected to the -6V line by the inversion switch, so that the voltage across either half of the transformer primary winding is equal in magnitude to the input voltage at all times, with the polarity reversing quickly and regularly.

Diodes D_1 and D_2 prevent coupling between the various long-pulse isolators. The transformer secondary feeds a full-wave rectifier to reconstitute the input to the isolator, modified slightly by the imperfections in diodes and transformer.

The forward voltage drops across the diodes reduce the output voltage of the unit by almost equal amounts whether the input is large or small, so almost suppressing the output when the input is small, and reducing it by a small fraction when the input is large.

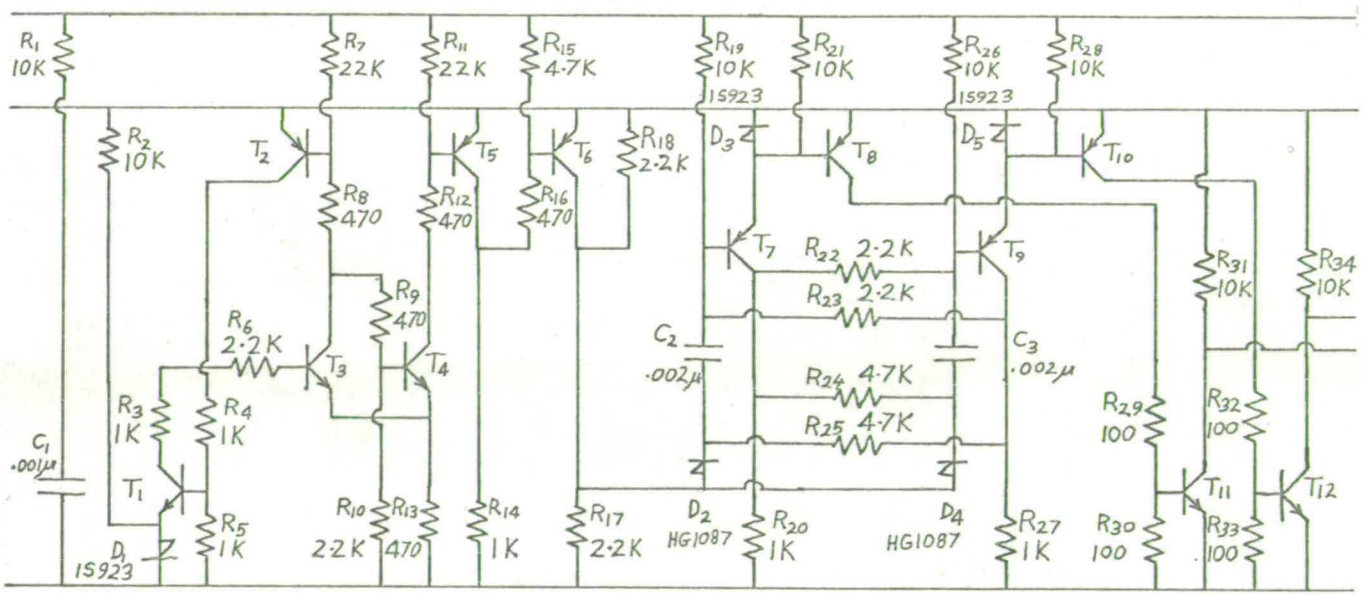
The transformer winding is quadrifilar to minimize leakage inductances. Magnetization built up during one part of an inversion cycle, may be accommodated during its decay by the load circuit, when this has low impedance, or through lines L_1 and L_2 by the inversion-switch circuit when the load has high impedance.

2.5.3 Inversion Switch

A pulse generator (Fig.2.5.3.) switches a bistable circuit regularly and thus controls the switching of transistors connecting lines L_1 and L_2 to the -6V supply.

The pulse generator is similar to the clock-pulse generator with a simplified input circuit for fixed-frequency operation, and an inverter at the output to reverse the polarity of the pulses.

ALL PNP TRANSISTORS 2N3702, ALL NPN...2N3704



The pulse-generator output is coupled to the bases of the bistable circuit transistors T_7 and T_9 through series diodes and capacitors; the latter are charged through resistors from the bistable outputs so that associated diodes are respectively forward or reverse biased during a clock pulse, and the pulse is fed only to the transistor due to receive it.

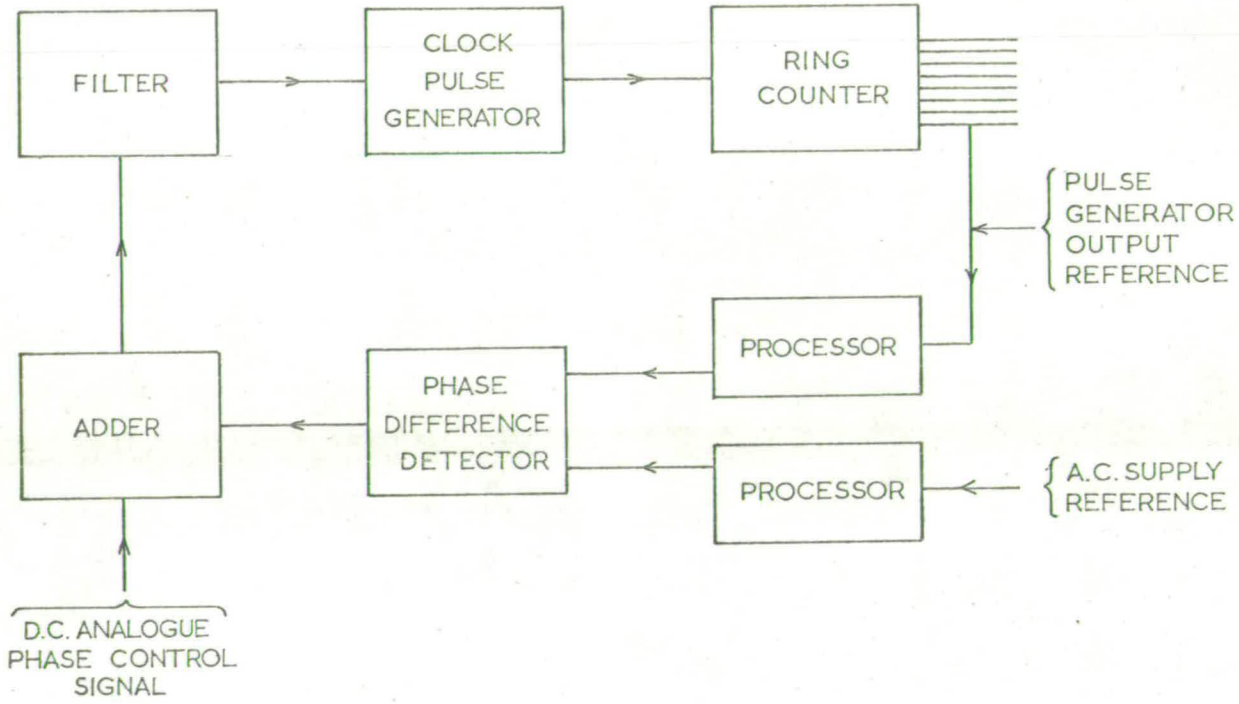
Transistors T_8 and T_{10} are controlled by the emitter currents of the bistable transistors and switch in unison with them. T_8 and T_{10} control the base currents of T_{11} and T_{12} respectively, these couple lines L_1 and L_2 to the -6V supply line. T_8 and T_{10} provide current amplification and the coupling circuit between these and T_{11} and T_{12} is a convenient point at which to introduce "speed-up" capacitors if necessary.

Power fed into the inversion switch by the isolating transformers is absorbed by transistors T_{11} and T_{12} by conduction at the collector breakdown voltage of each transistor at the start of its "off" period.

2.6 Phase-Control Circuit

The scheme is shown in Fig. 2.6(a). A reference voltage at supply frequency and another at pulse-generator output frequency are fed to a phase-detector circuit. This produces a phase-difference signal which is added to a control signal, filtered, and fed to the clock-pulse generator to control its output frequency.

Both reference signals are converted to a succession of short pulses by suitable processing, and the phase-difference detector is a simple digital circuit.


FILTER
CLOCK PULSE GENERATOR
RING COUNTER
PULSE GENERATOR OUTPUT REFERENCE
PROCESSOR
ADDER
PHASE DIFFERENCE DETECTOR
PROCESSOR
A.C. SUPPLY REFERENCE
D.C. ANALOGUE PHASE CONTROL SIGNAL

2.6(a)

The complete phase control circuit is shown in Fig. 2.6(b), and the operation of its various parts is explained in the following sections.

2.6.1 Pulse Generator Reference Processor

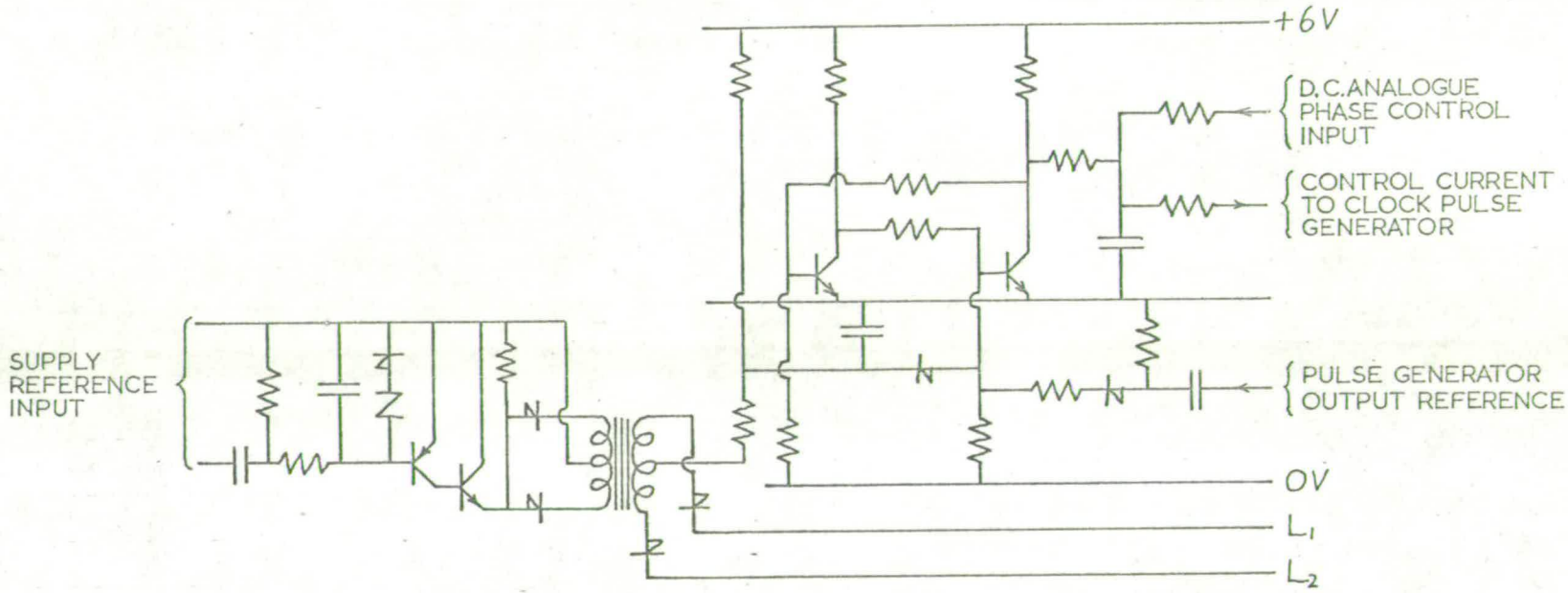
In Fig.2.6.1, digital signals from the pulse generator are differentiated by capacitor C and resistor R, then negative going pulses are fed forward to the phase-difference detector through diode D.

2.6.2 Supply Reference Processor

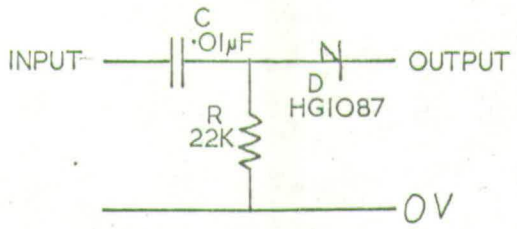
The incoming reference voltage v_1 is applied to the input of the filter, Fig.2.6.2, comprising R_1 C_1 R_2 C_2 loaded by the base-emitter junction of T_1. C_1 blocks the direct component of the input voltage; the alternating component is applied to R_2 and C_2 in series, so that the integral v_2 of v_1 is applied across the base-emitter junction of T_1. This non-linear load clamps v_2 to values more negative than a small positive voltage. During most of the input cycle, v_2 is not clamped, and is the integral of v_1; at positive peaks of v_2, the base-emitter junction of T_1 carries a short pulse of current i_2. This turns on T_1 to switch a load on to the d.c. supply. Transistor T_2 provides current amplification.

2.6.3 Isolation

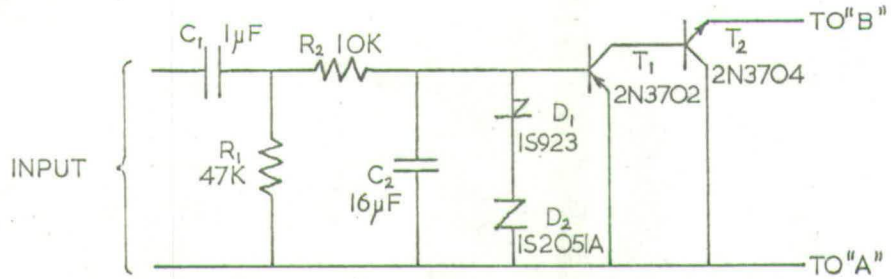
The circuit shown in Fig.2.6.3 isolates the supply reference processor from the phase-detector circuit. The system of feeding the two halves of the primary winding of a transformer through the inversion switch is used, as in section 2.5.2, to feed a d.c. signal from one circuit to another with electrical isolation between the two circuits.


+6V
D.C.ANALOGUE PHASE CONTROL INPUT
CONTROL CURRENT TO CLOCK PULSE GENERATOR
SUPPLY REFERENCE INPUT
PULSE GENERATOR OUTPUT REFERENCE
0V
L1
L2

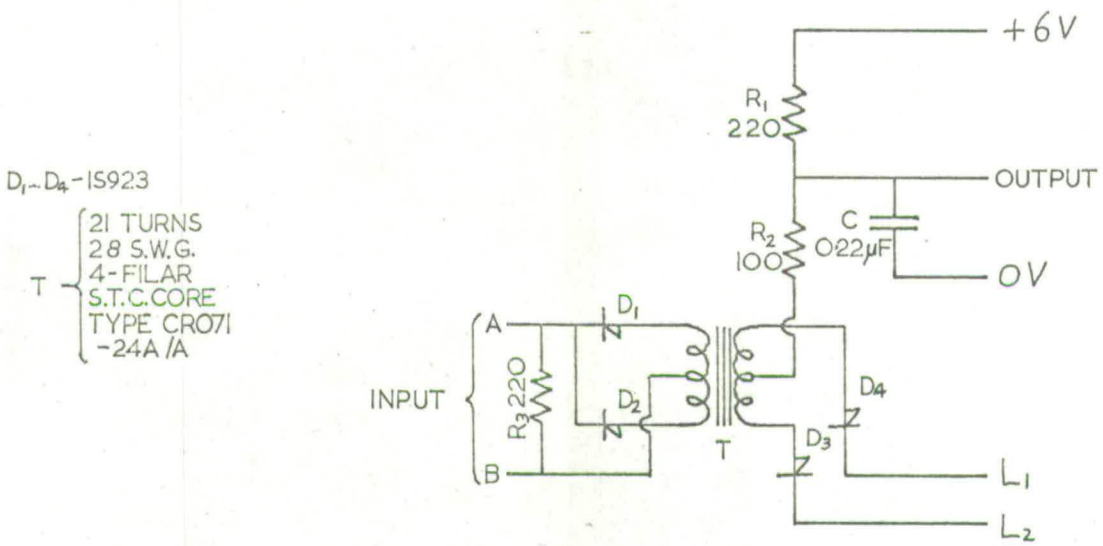
2.6(b)


C
·01μF
INPUT
OUTPUT
D
HG1087
R
22K
0V

2.6.1


C1 1μF
R2 10K
TO "B"
T2
2N3704
T1
2N3702
D1
1S923
INPUT
R1
47K
C2
16μF
D2
1S2051A
TO "A"

2.6.2


D1 - D4 - 1S923
T
21 TURNS
28 S.W.G.
4-FILAR
S.T.C. CORE
TYPE CR071
-24A/A
+6V
R1
220
OUTPUT
R2
100
C
·022μF
0V
A
D1
INPUT
R3 220
D2
D4
T
D3
B
L1
L2

2.6.3

The supply reference processor loads the transformer through the rectifier D_1, D_2, and changes in load are sensed as voltage changes across resistor R_1 in series with the power supply to the transformer. Resistor R_2 makes the d.c. output levels correspond to those required; capacitor C shunts carrier-frequency currents to earth and diode D_5 prevents the isolator from interfering with the bistable action of the phase-difference detector.

2.6.4 Phase Difference Detector

In Fig.2.6.4 NPN transistors T_1 and T_2 are in a bistable circuit; negative going supply reference pulses and positive going pulse generator reference pulses are fed to the base of T_1, so that the latter is switched off by pulses from one source and on by pulses from the other.

The output is taken from the collector of T_1; when the two pulse trains are in synchronism, the mark to space ratio of the output voltage v_o is a function of the phase difference between the two, and the mean value of v_o is proportional to the lag of pulse generator derived pulses relative to supply derived pulses.

2.6.5 Adder and Filter

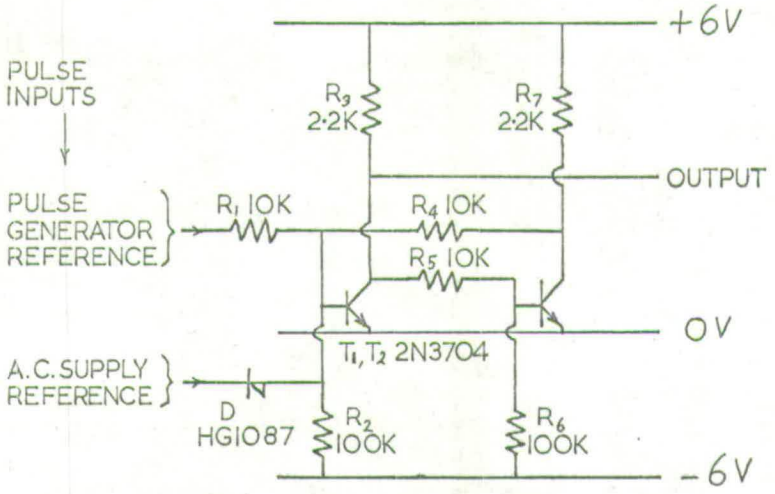
The current i_o (Fig.2.6.5) fed forward is related to the input voltages v_1 and v_2 by the following equation:

$$i_o = Av_1 + Bv_2$$

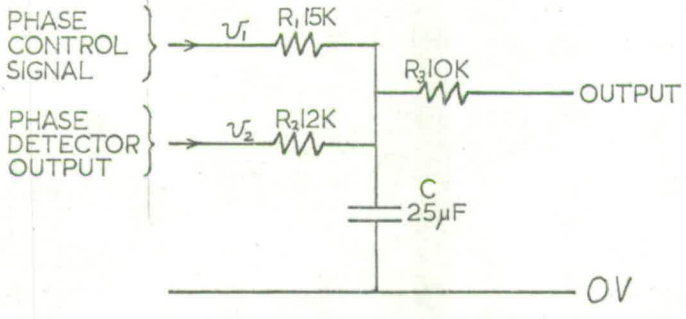
where i_o, v_1 and v_2 are mean values

and A and B are circuit constants derived in Appendix 1.

Capacitor C conducts in proportion to the rate of change of i_o, so that the circuit performs as would an adder followed by a filter.


+6V
PULSE INPUTS
R3 2·2K
R7 2·2K
OUTPUT
PULSE GENERATOR REFERENCE
R1 10K
R4 10K
R5 10K
0V
T1, T2 2N3704
A.C. SUPPLY REFERENCE
D HG1087
R2 100K
R6 100K
-6V

2.6.4


PHASE CONTROL SIGNAL
V1
R1 15K
R3 10K
OUTPUT
PHASE DETECTOR OUTPUT
V2
R2 12K
C 25μF
0V

2.6.5

CHAPTER 3

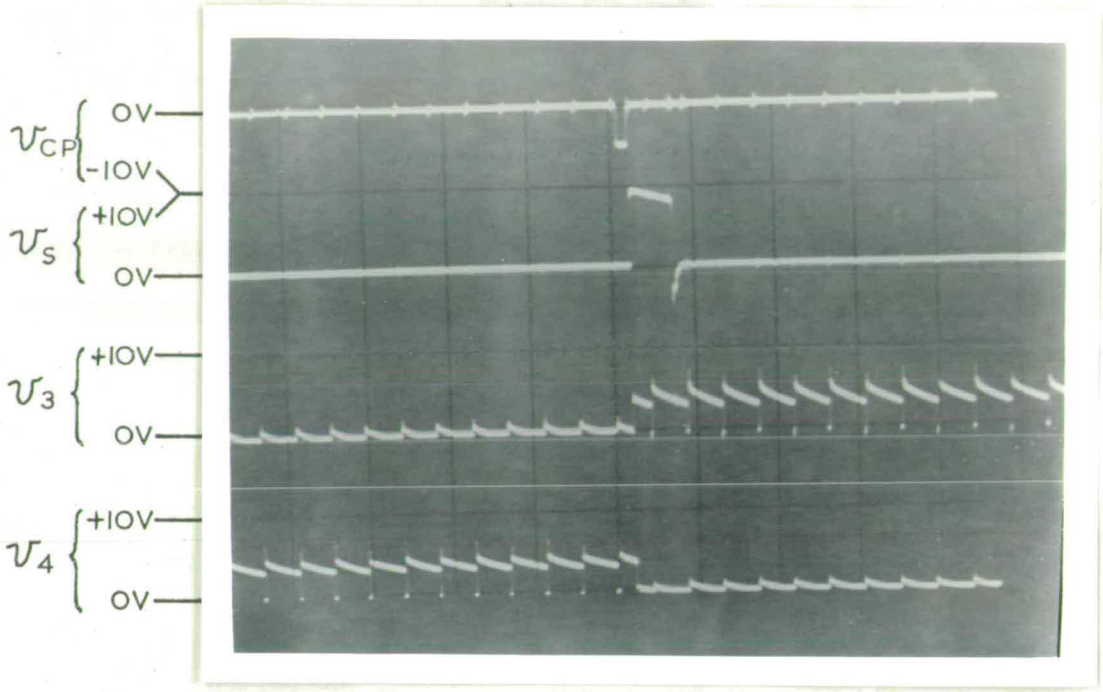
PERFORMANCE OF UNIT

During construction each stage was tested and the design checked; each stage operated as planned. The following sections of this chapter display and discuss the operation of the complete unit, its frequency and phase responses and internal operation.

3.1 Gate-Voltage Waveform

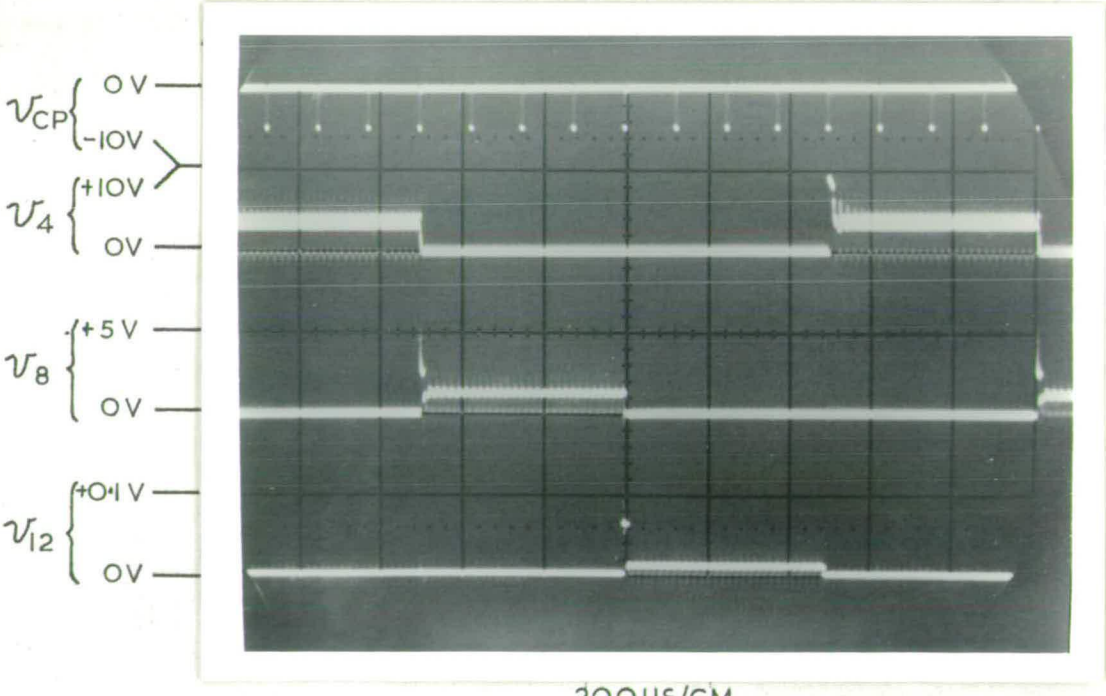
The top trace of Fig.3.1(a) shows the clock pulse waveform v_{cp}; at the termination of the clock pulse the short output pulse v_s is initiated, shown in the second trace; this is abruptly terminated after 10μs. The bottom two traces v_3, v_4 show long output pulses; one of these is initiated and the other terminated at the start of the short pulse, corresponding to one thyristor receiving firing and holding pulses (v_s and v_3) while the holding supply v_4 of another thyristor is terminated.

Short output pulses have trapezoidal shape, and long output pulses are composed of a succession of trapezoidal blocks separated by 0.5μs gaps; the falling amplitude of the waveforms is caused by the short time constant of the primary circuit of the isolating transformers, arising in turn from the position of the droop resistor in the primary circuit of each output transformer; this allows the initial short circuit output current of each stage to be nearly equal to the maximum rated value for the appropriate switching transistor, and the position of the isolating transformer at the low voltage side of the resistor minimises magnetisation in this component.



20 μs/CM

3.1(a)



200μs/CM

3.1(b)

Rise time of short output pulses is approximately 20 ns, giving virtually ideal thyristor gate firing. A reverse voltage spike of very short duration occurs at short pulse termination, caused by finite reverse recovery time of the diode which blocks transformer resetting voltage; the charge transmitted is very small and should therefore have little effect on thyristor operation. Gaps in the long pulse waveform are caused by the finite reverse recovery time of diodes in the isolation circuit or by slightly overlapping "off" or "on" periods of the inversion switch transistors.

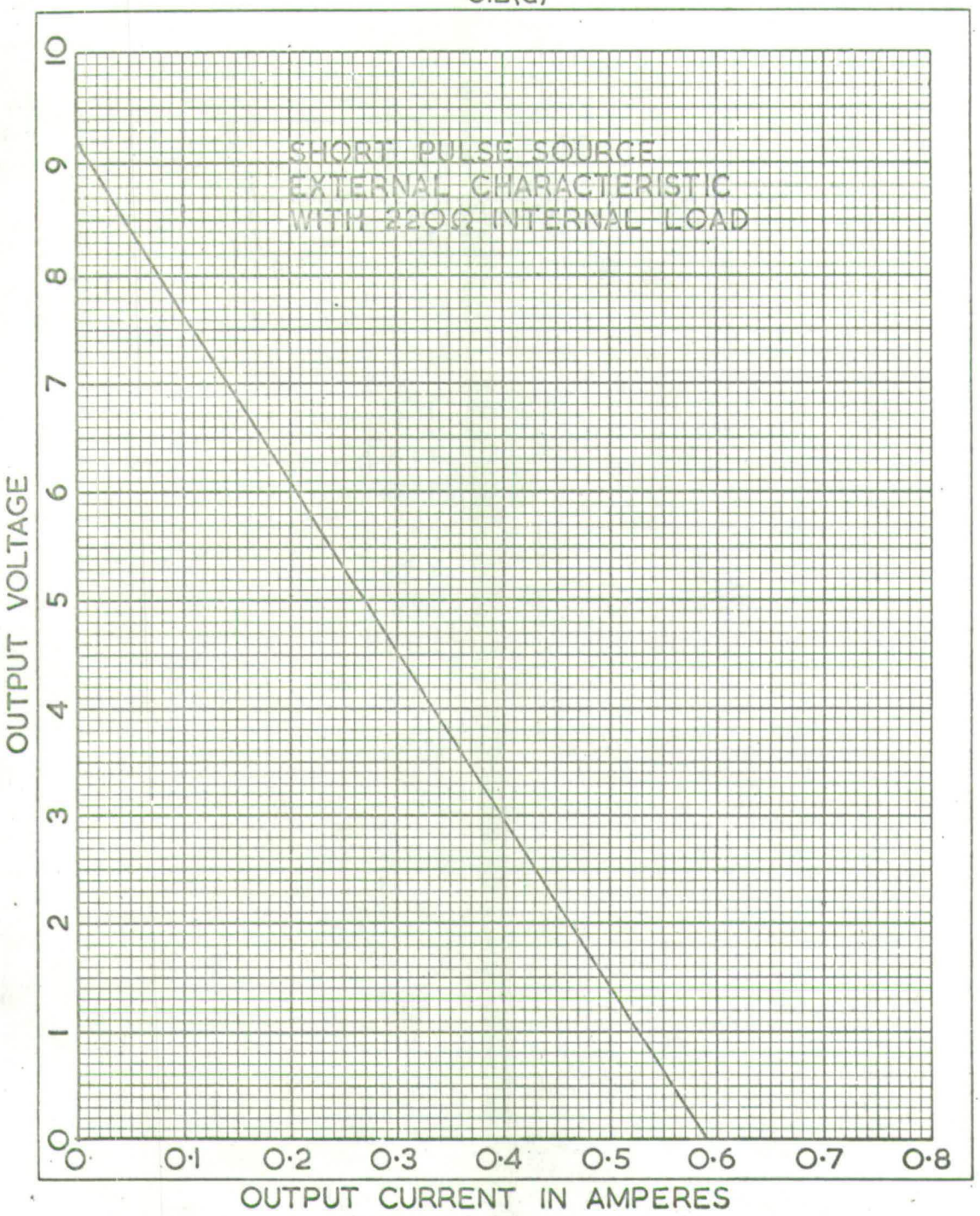
The traces of Fig.3.1(b) illustrate a number of features of the outputs fed to one ring of 3 thyristors. Recurrent operation of any one gate conforms to each 12th clock pulse; each gate conducts over 4 clock periods; the 3 gates conduct in sequence.

In the oscillogram each output had a different load to illustrate loaded operation of the system. Output No.4, trace 2 is virtually open circuit; comparison with Fig.3.1(a) shows the short reverse voltage spike produced by the short pulse generator to have been eliminated by connection of short and long pulse generators in parallel. Trace 3 shows the effect of thyristor gate loading and trace 4 (at bottom) shows the effect of 0.1_{Ω} resistive load, virtually a short circuit. This latter load reduces the output voltage nearly to zero, so that magnetisation of the output transformer is very small, and the output pulse is rectangular.

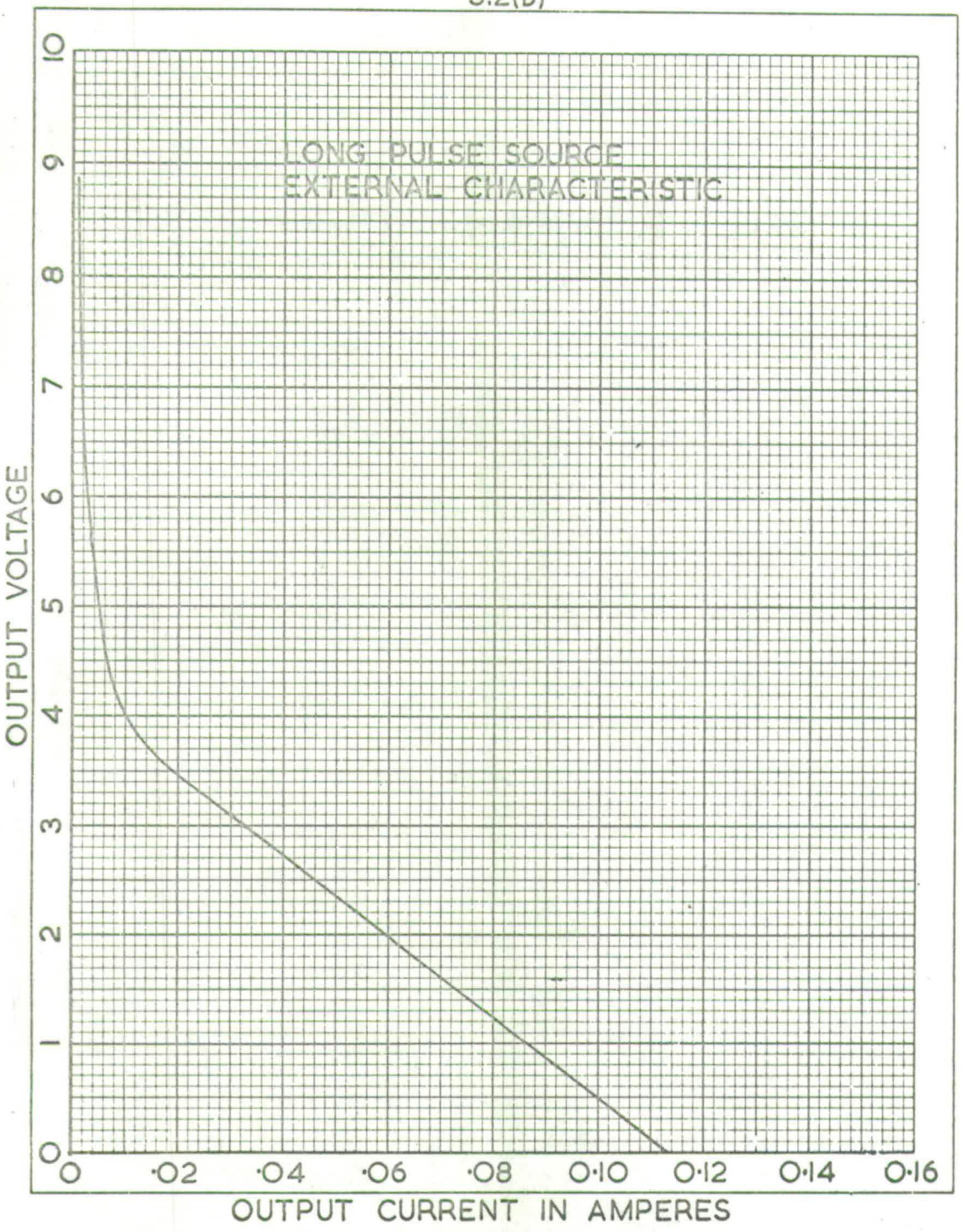
3.2 Load Characteristics

Load characteristics of the short and long pulse generators were measured and are shown in Figs. 3.2(a) and (b) respectively.

3.2(a)


SHORT PULSE SOURCE
EXTERNAL CHARACTERISTIC
WITH 220Ω INTERNAL LOAD
OUTPUT VOLTAGE
0
1
2
3
4
5
6
7
8
9
10
0
0·1
0·2
0·3
0·4
0·5
0·6
0·7
0·8
OUTPUT CURRENT IN AMPERES

3.2(b)


LONG PULSE SOURCE
EXTERNAL CHARACTERISTIC
OUTPUT VOLTAGE
0
1
2
3
4
5
6
7
8
9
10
0
·02
·04
·06
·08
0·10
0·12
0·14
0·16
OUTPUT CURRENT IN AMPERES

These characteristics permit the pulse system to be married to any particular thyristor. The straight line short pulse characteristic and the straight line part of the long pulse characteristic arise from the resistive part of the internal impedance. The greatly increased output voltage with very light loads arises when instantaneous power fed from long pulse source to long pulse isolation circuit becomes zero at any part of the inversion cycle; this occurs at finite mean output power because of cyclically varying transformer magnetisation. This is not a practical disadvantage, as a fairly high resistance connected in parallel with the load will give a completely linear load characteristic.

3.3 Frequency Control

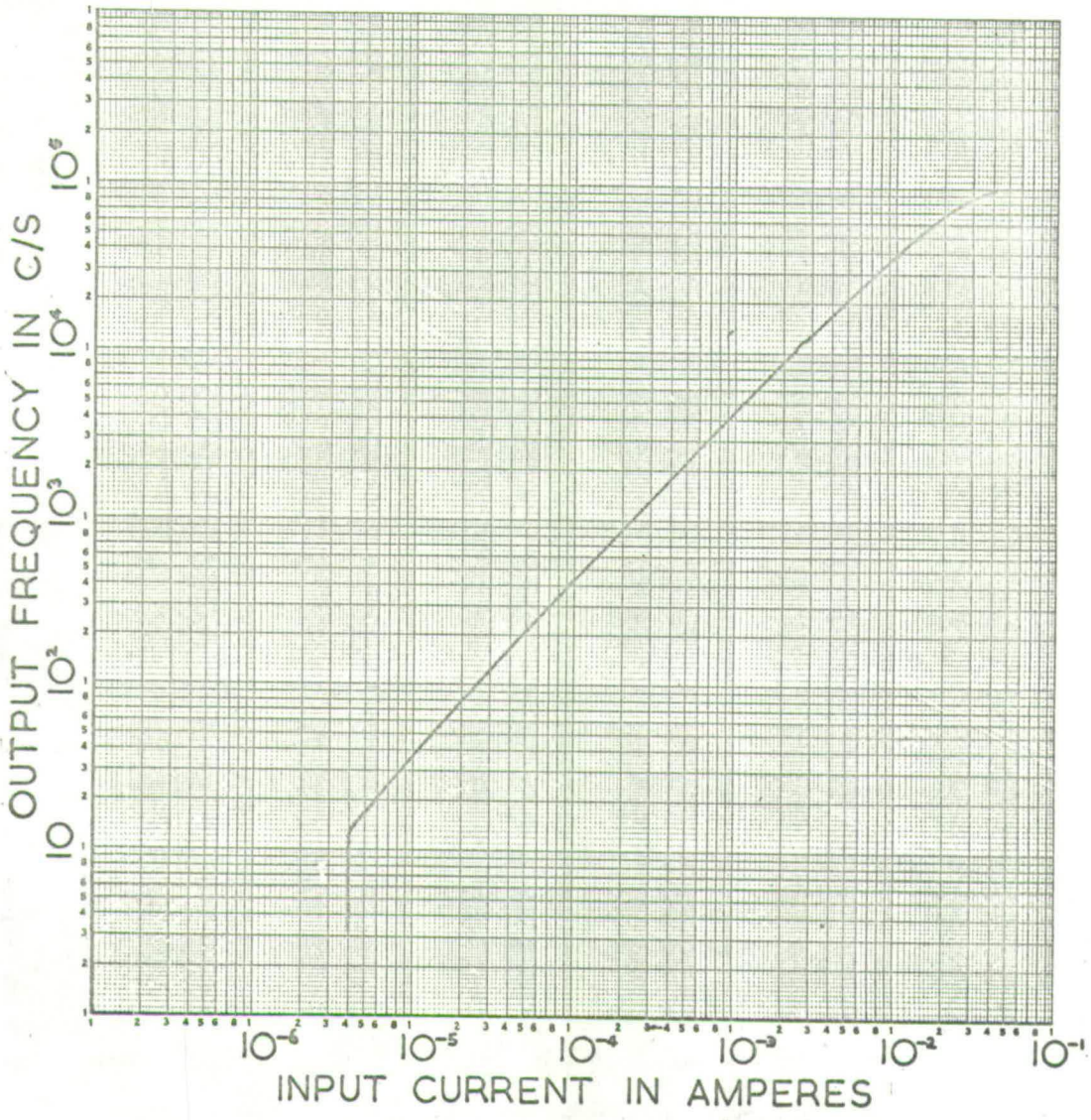
Clock pulse frequency against input control current has been measured and is shown in Fig.3.3(a). Pulse generator output frequency is 1/12 clock pulse frequency. Current control is approximately linear from 20 c/s to 40 kc/s (clock pulse frequency) with improved linearity over a narrower range between these limits. The frequency range may be changed quite simply.

The input characteristic is shown in Fig.3.3(b); this is non linear, but the input voltage is quite low and nearly constant, giving a good approximation to a virtual earth. Resistors connected from the pulse generator input to fixed and variable voltage sources may be used to give fixed and variable components of output frequency.

Voltage control of frequency is illustrated by Fig.3.3.(c) in which control voltage and output frequency are plotted against

3.3(a)

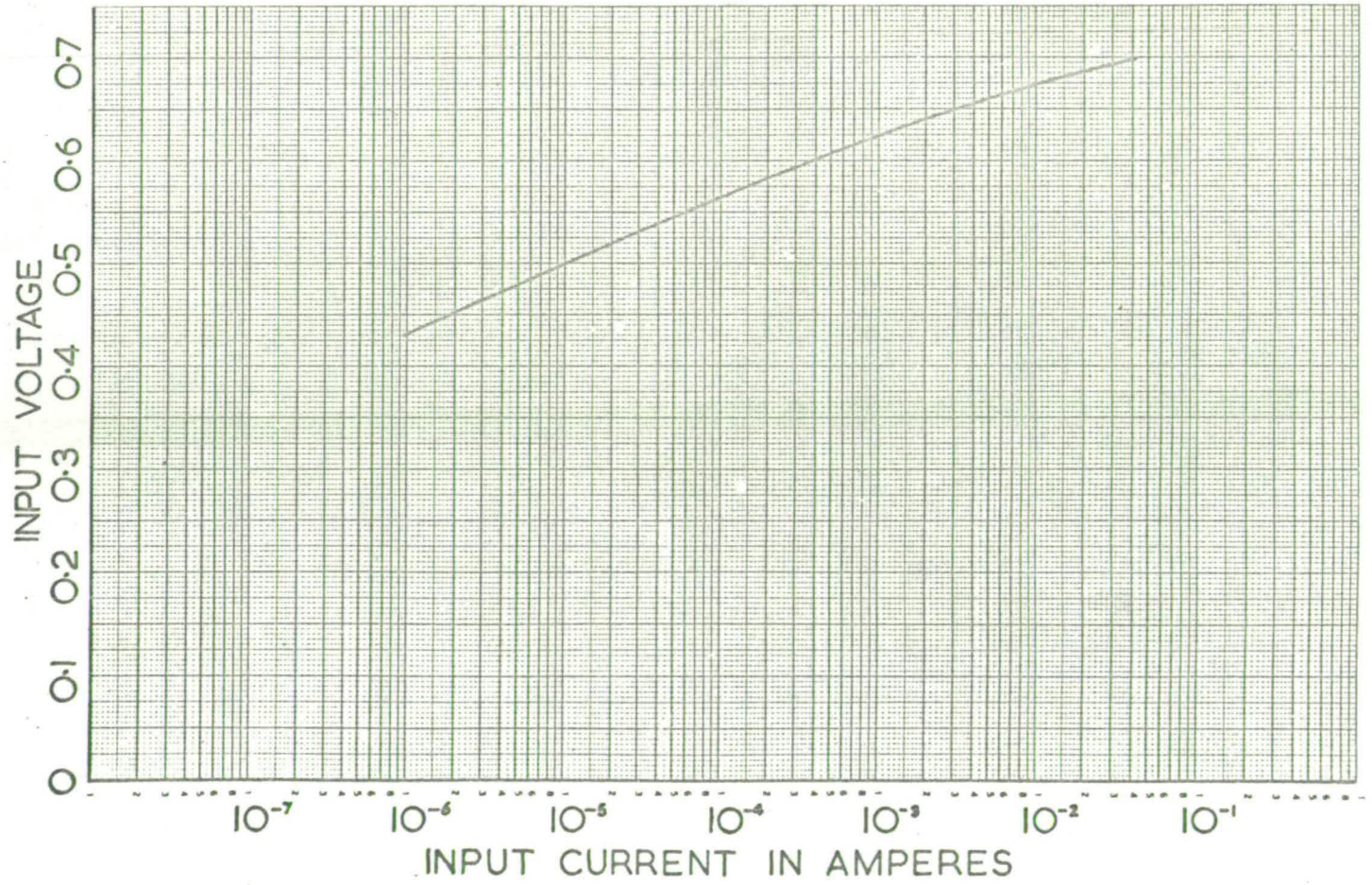
CLOCK PULSE GENERATOR
CONTROL CHARECTERISTIC

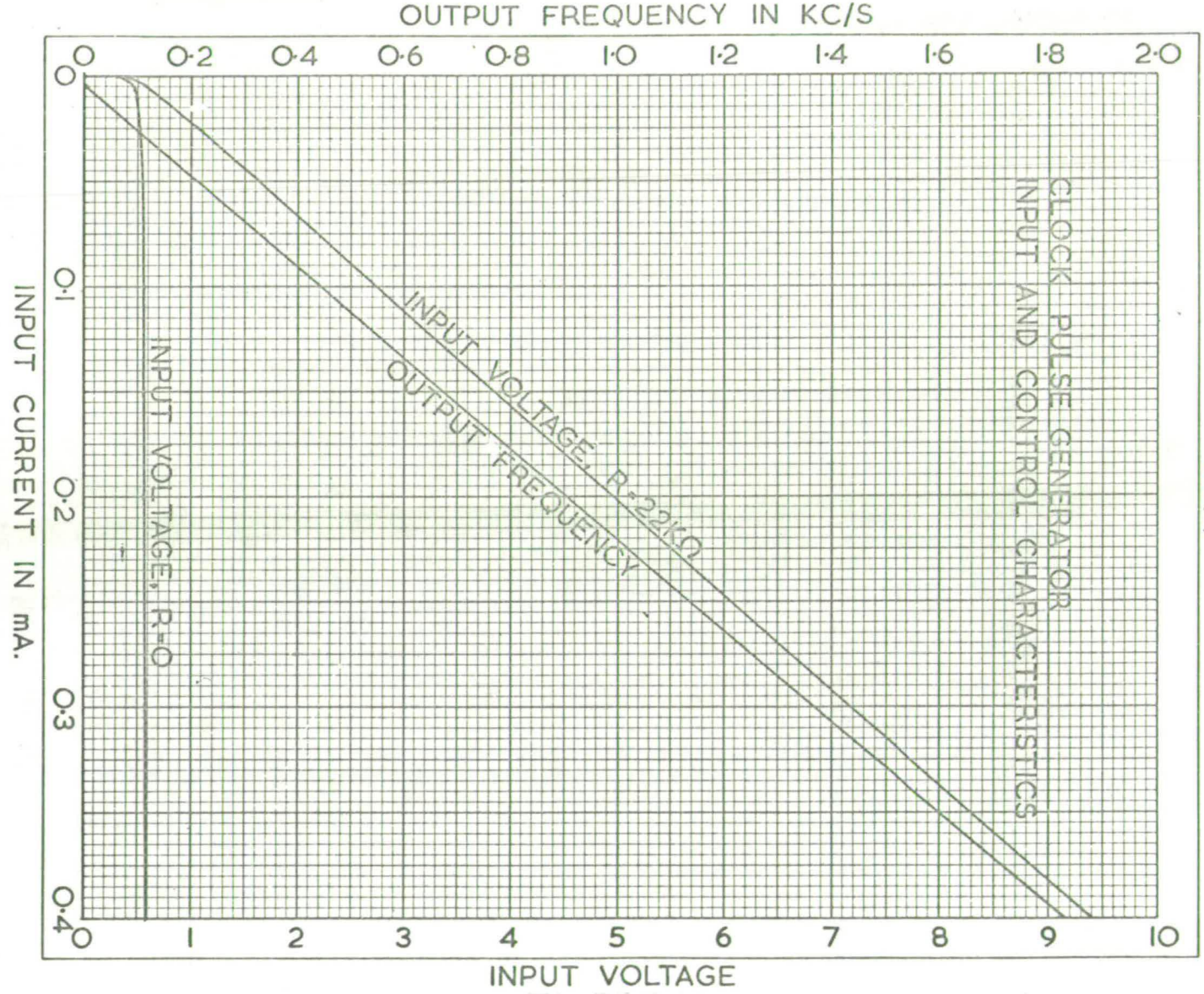


CHARTWELL GRAPH SHEET No. 5781 LOG 8 CYCLES X MM., ½ & 1 CM.

3.3(b)

CLOCK PULSE GENERATOR INPUT CHARACTERISTIC




OUTPUT FREQUENCY IN KC/S
0
0·2
0·4
0·6
0·8
1·0
1·2
1·4
1·6
1·8
2·0
0
0·1
0·2
0·3
0·4
INPUT CURRENT IN mA.
INPUT VOLTAGE, R=0
INPUT VOLTAGE, R=22kΩ
OUTPUT FREQUENCY
CLOCK PULSE GENERATOR
INPUT AND CONTROL CHARACTERISTICS
0
1
2
3
4
5
6
7
8
9
10
INPUT VOLTAGE

3.3(c)

control current. Control voltage is shown for zero and finite series input resistance, showing linearity of voltage control of frequency using series input resistance.

3.4 Synchronous Running

The pulse generator output frequency is zero with zero control current; synchronous operation is brought about by application of finite current, with constant correction to maintain synchronism.

Positive control current is derived by a passive loop filter from two positive voltage sources; one of these is the phase detector and the other is the control source. Change of control voltage causes change of output frequency; this ultimately changes output phase, leading eventually to restored balance with different output phase.

The loop filter smooths the pulse generator control signal to ensure nearly equal conduction angles of all 12 thyristors; smoothing is by single RC integration, giving the simplest possible system.

Pull-in to synchronism is assured by application of the control voltage which at synchronism would give steady running in the centre of the linear phase detector characteristic. While the pulse generator frequency is below supply frequency, the mean current fed to the filter is in excess of the value at synchronism, so that acceleration takes place as the filter capacitor becomes charged. Once synchronism has been reached, phase overshoot is within the phase detector linear limits and finite damping assures

the stability of the condition. With very low damping (large filter capacitor) synchronous speed is not reached with slightly diminished control voltage, and slightly excessive control voltage gives overshoot leading to operation above synchronous speed.

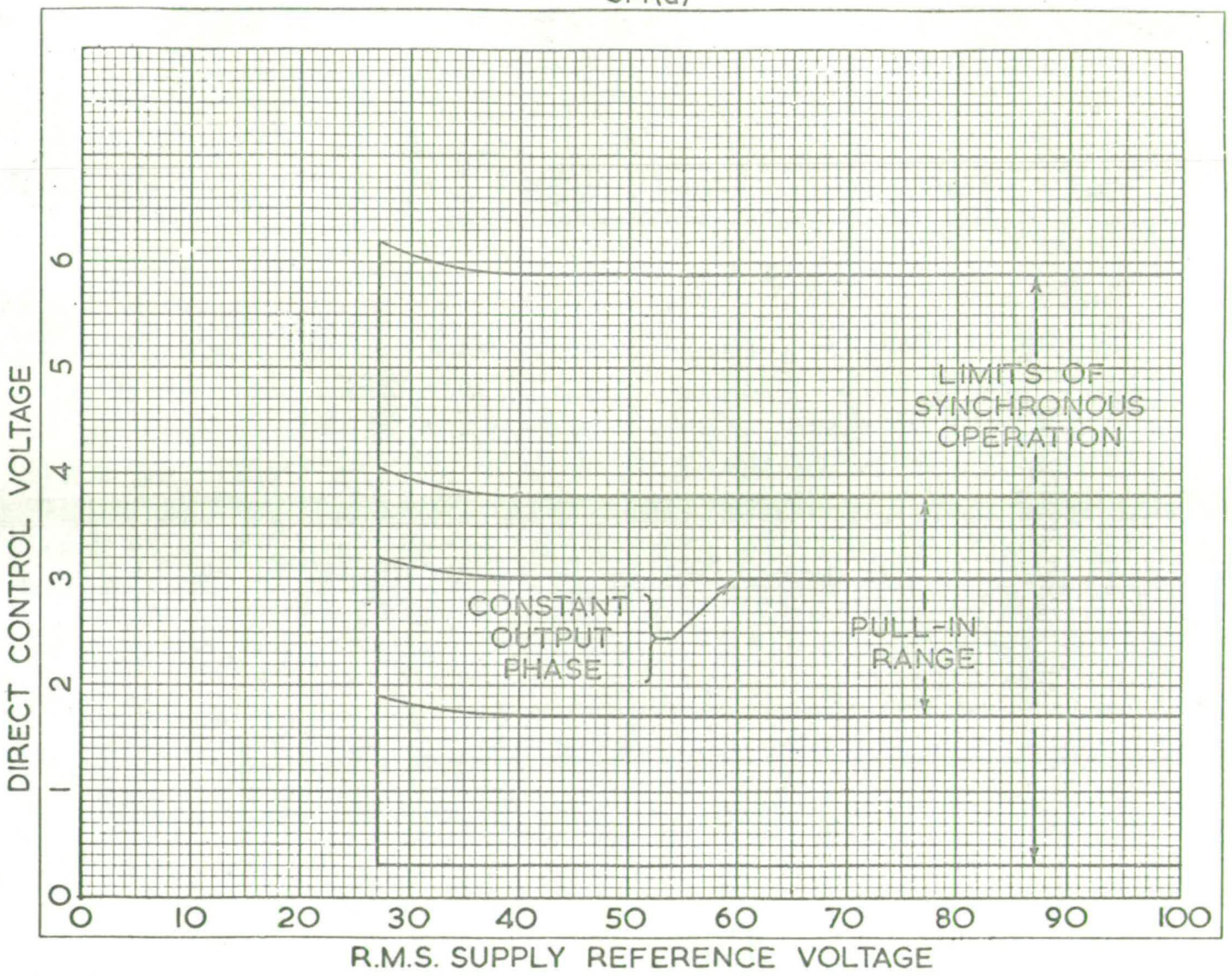
The normal damping ratio gives synchronisation within the "pull-in" range shown in Fig.3.4(a); operation within the pull-in range will ultimately result in synchronisation. This is in qualitative agreement with conventional phaselock theory, which states that increase of loop bandwidth gives increase of pull-in range.

When synchronism has been achieved, slow changes of control voltage between the "limits of synchronous operation" shown in Fig.3.4(a) will not give loss of synchronism.

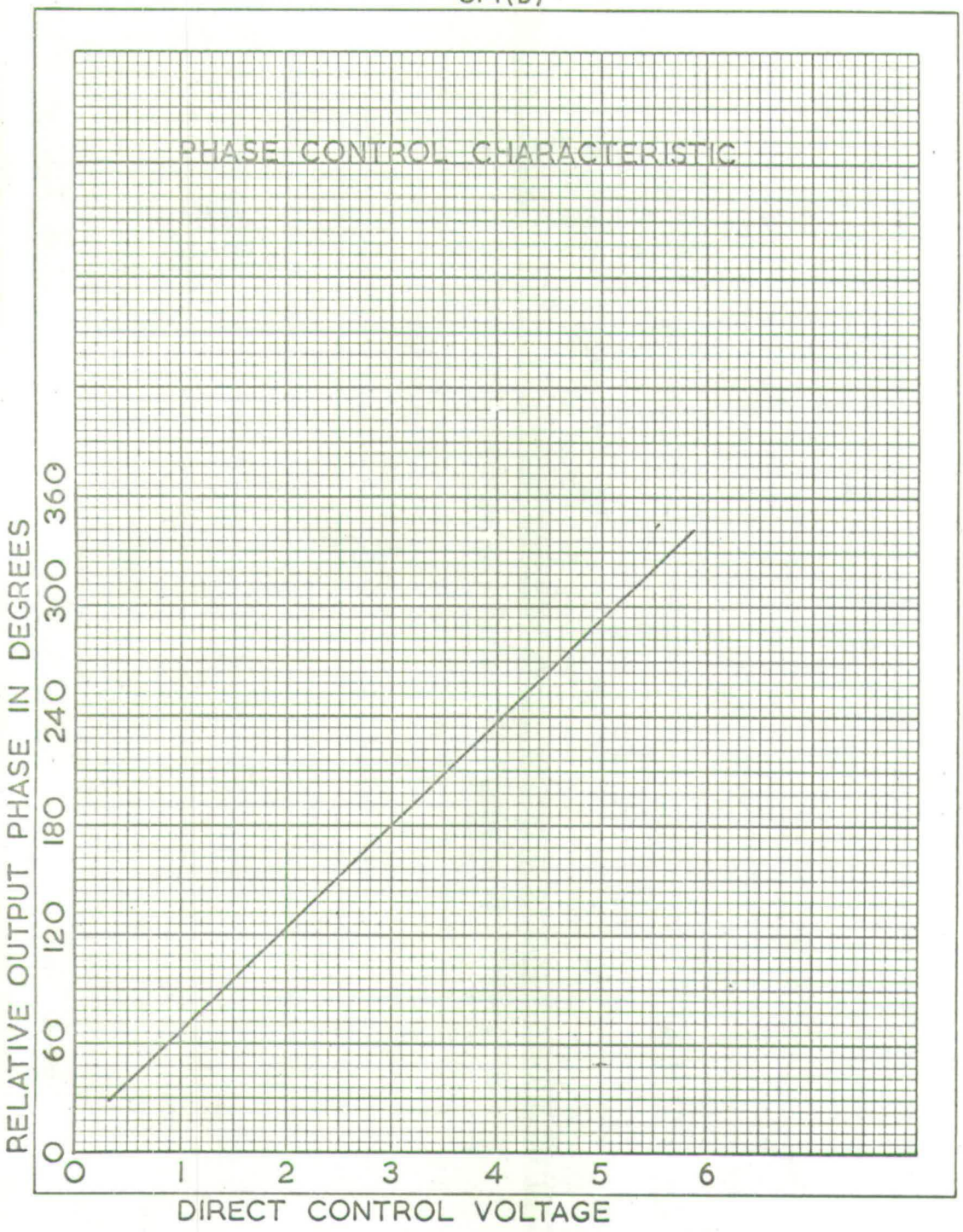
Fig.3.4(a) also shows the excellent static performance of the supply reference processor (section 2.6.2); variation of supply voltage amplitude has very little effect on pulse generator phase and pull-in range and limits of synchronous operation. The central nearly horizontal line is a locus of constant pulse generator phase.

The linear phase detector characteristic gives linear voltage control of phase. This is shown in Fig.3.4(b) in which control voltage is plotted at precise 30^{o} increments in phase by bringing each of the 12 thyristor gate signals in turn into a given phase relationship with the supply. A family of curves at 30^{o} intervals is obtained by using different pulse generator output phases to supply reference digits to the phase control circuit; only one such curve is shown. Static control rate is 0.8075 volts/radian, but sensitivity may easily be altered to suit specific requirements.

3.4(a)


DIRECT CONTROL VOLTAGE
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
80
90
100
R.M.S. SUPPLY REFERENCE VOLTAGE
LIMITS OF SYNCHRONOUS OPERATION
CONSTANT OUTPUT PHASE
PULL-IN RANGE

3.4(b)

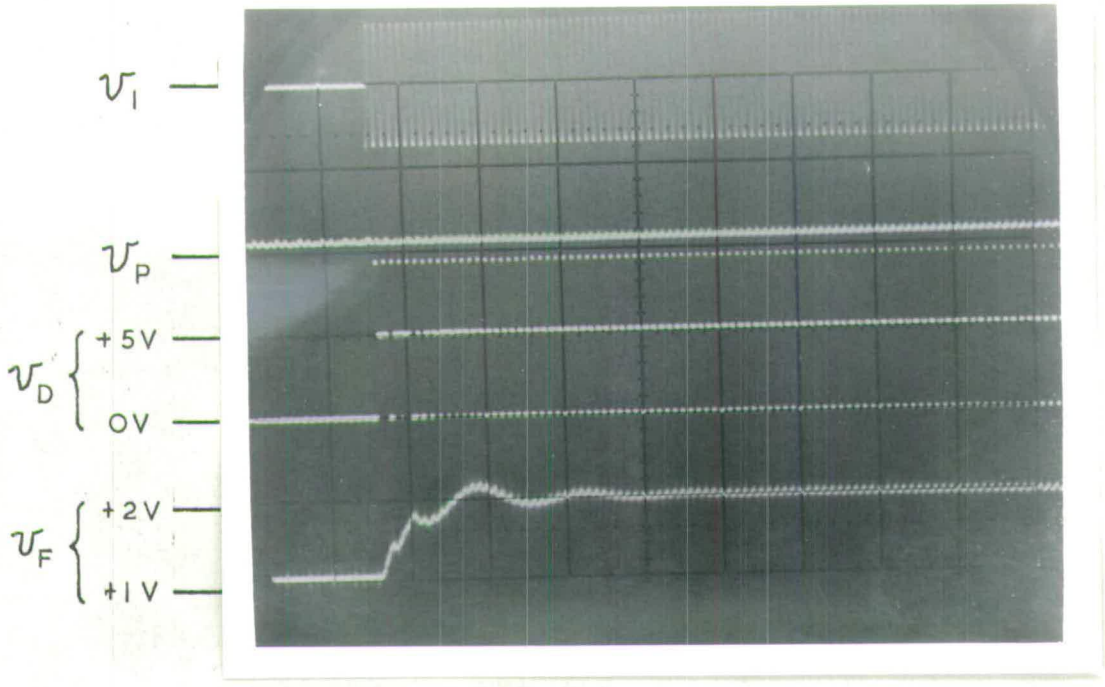

PHASE CONTROL CHARACTERISTIC
RELATIVE OUTPUT PHASE IN DEGREES
0
60
120
180
240
300
360
0
1
2
3
4
5
6
DIRECT CONTROL VOLTAGE

3.4.1 Dynamic Response

The dynamic behaviour of the phaselock loop was tested by taking oscillograms of the principal voltage waveforms during pull-in and subsequent phase and frequency transients. The ringing which occurs in the synchronised condition is related to system parameters by simple formulae; these are used to confirm that the circuit works as planned.

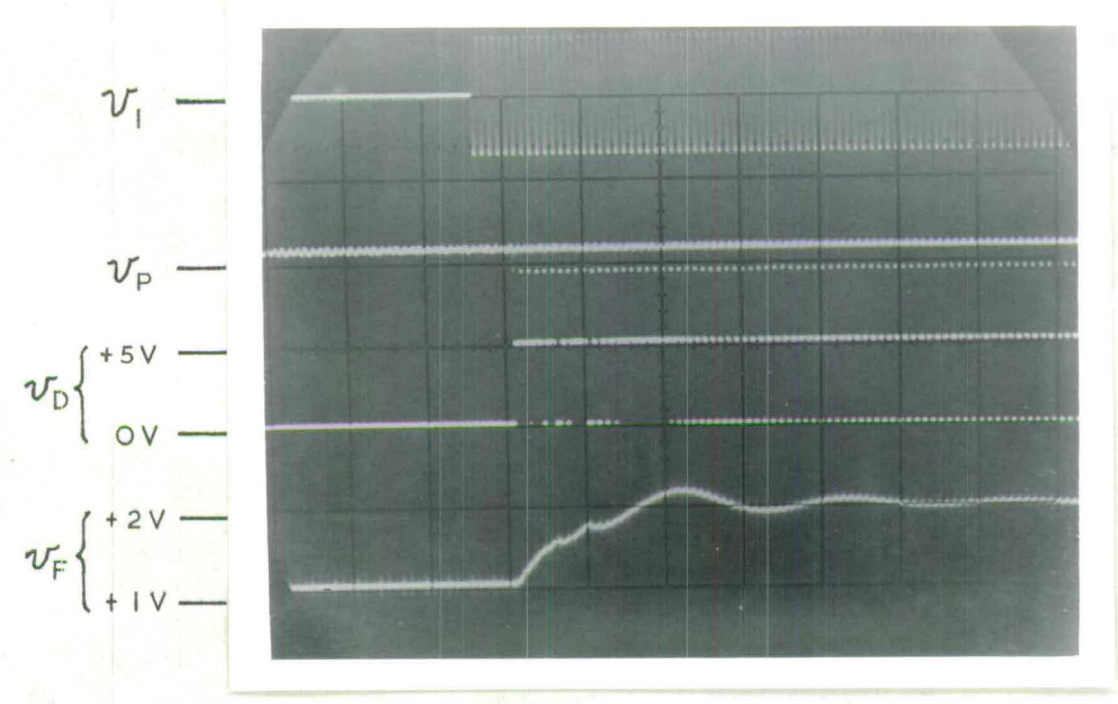
Fig.3.4.1(a) shows synchronisation by the sudden application of supply reference voltage; top trace shows supply reference at a scale of 100 V/cm, second trace shows pulses v_p derived from the supply reference by the unit described in section 2.6.2. Third trace is of phase detector output v_d; this has digital form, being switched to +6V by the supply reference pulses v_p and to 0V by the pulse generator output once per cycle. The mark to space ratio is therefore indicative of pulse generator phase relative to supply phase; the time scale of the oscillogram shows supply cycle time as a very short length, so that relative brilliancy of upper and lower parts of the trace indicate phase oscillations after synchronisation.

The fourth (bottom) trace shows filter capacitor voltage v_f which is approximately proportional to pulse generator output frequency. The exact relationship may be calculated from the clock pulse generator calibration curves and the resistance connected from filter capacitor to clock pulse generator input; it is nearly linear from zero frequency at v_f = 0.6V to 50 c/s at v_f = 2V.



0·2 S/CM

3.4.1(a)



0·2 S/CM

3.4.1(b)

It can be seen that pulse generator frequency rises rapidly from approximately 14 c/s until synchronisation occurs, indicated by the 1:1 relationship between the digits of v_p and v_d. Ringing of frequency (v_f) is apparent for approximately 0.6 sec, after which resonance is negligible.

Frequency ripple with triangular waveform is visible from synchronisation onwards; this is caused by integration of phase detector digits in the filter, and has acceptably low magnitude.

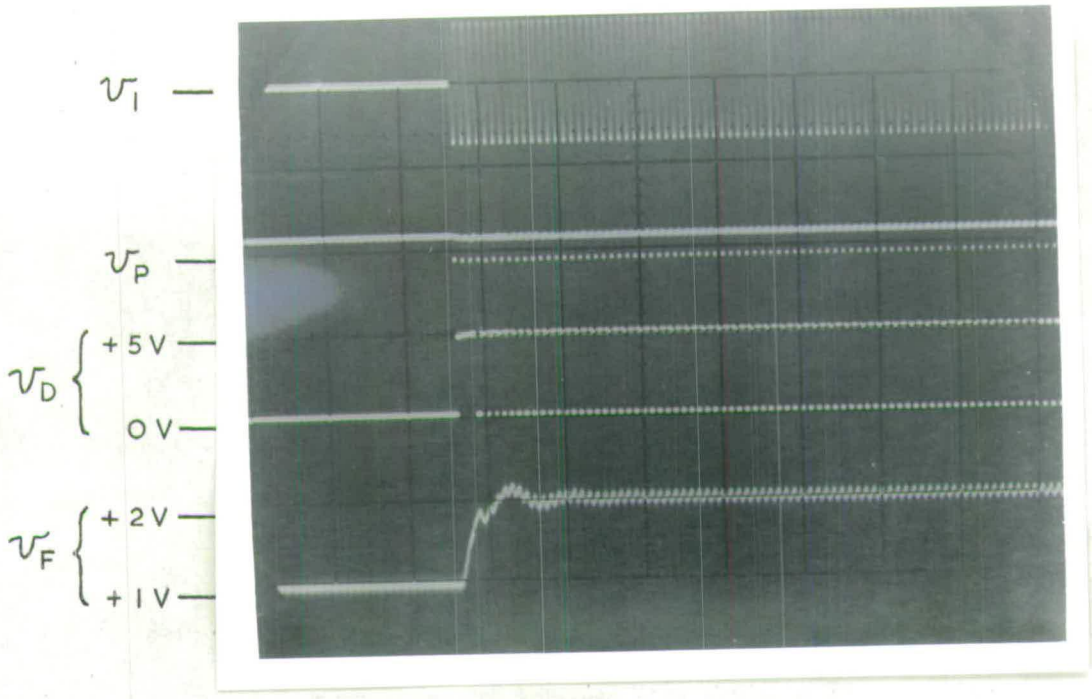
Figs.3.4.1(b) to (g) show the effect of varying filter parameters on synchronisation and transient response, and different methods of synchronisation. System resonant frequency and damping factor have been measured in each case and are tabulated for comparison with calculated values in Appendix 2.

(b) shows the effect of increasing filter time constant T_F to improve smoothing of the phase detector digits; system resonant frequency has been lowered and damping reduced, giving longer settling time; phase ringing (v_d) is now easily apparent.

(c) shows the effect of increasing loop gain K to give faster response; resonant frequency is raised and damping is increased, but frequency ripple (v_f) is increased.

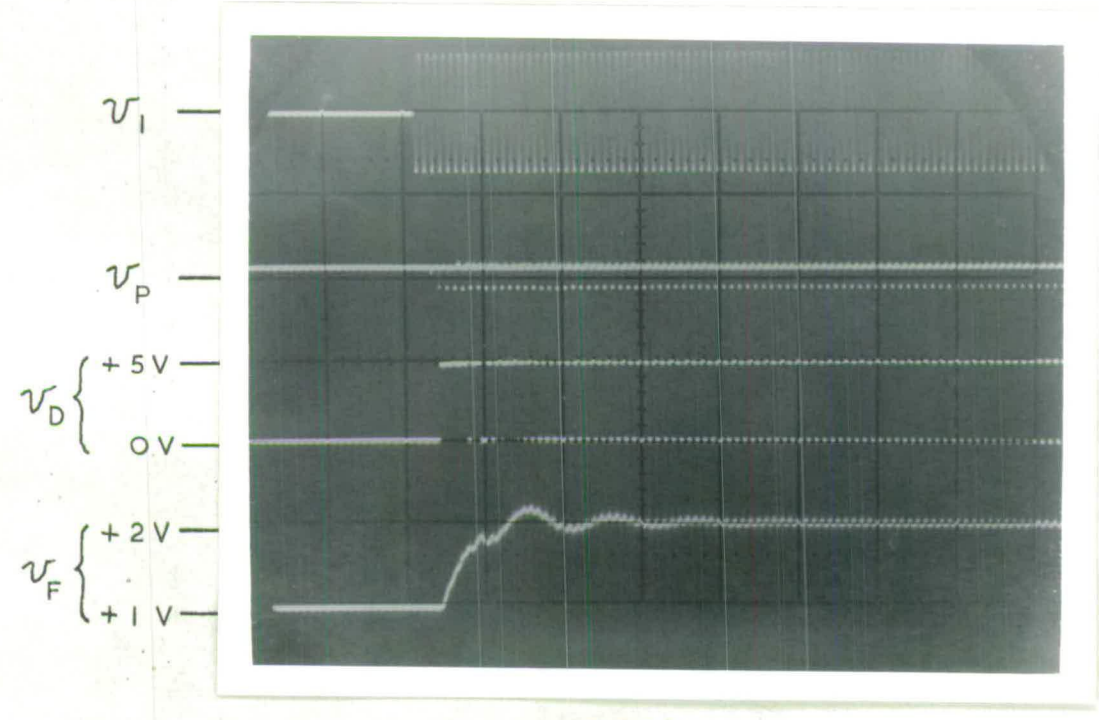
(d) shows the effect of increasing T_F to restore smoothing to the original level, whilst maintaining the high value of K as in (c). Resonant frequency is now still above the original value but ringing is more persistent so that settling time is similar.

(e) shows the effect of very low T_F and high K giving fast response with little ringing, and large frequency ripple.



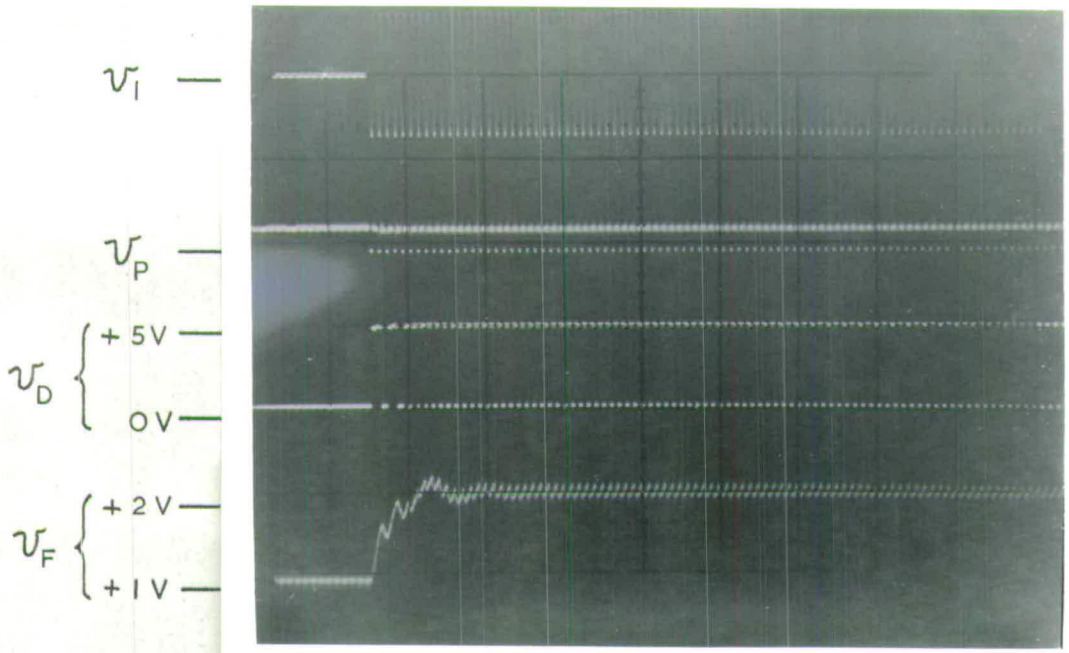
0·2 S/CM

3.4.1(c)



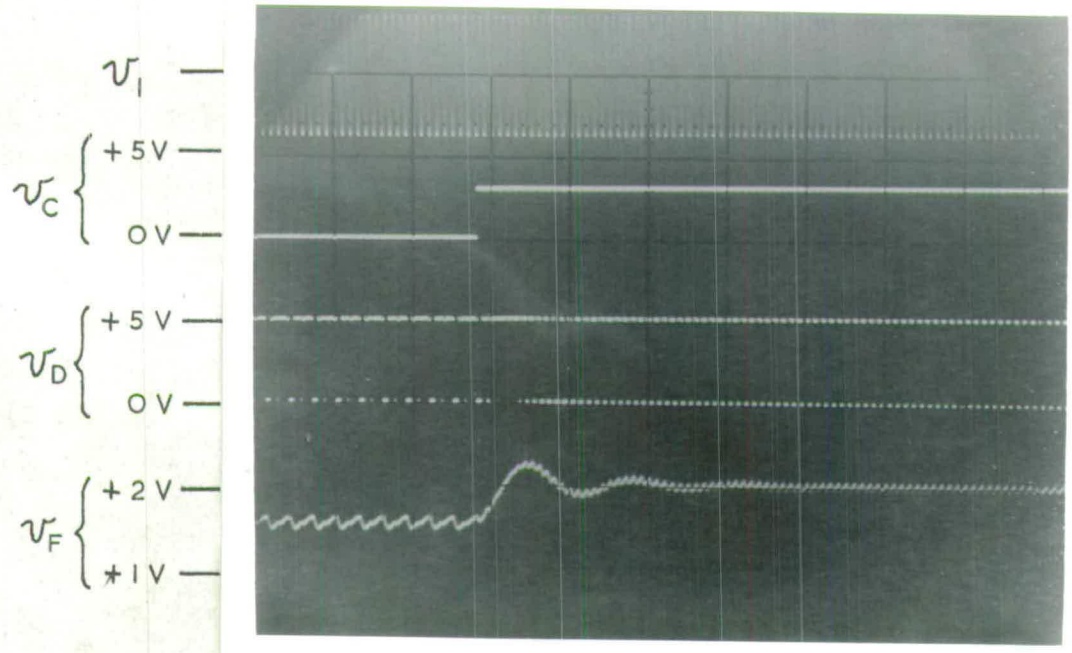
0·2 S/CM

3.4.1(d)



0·2 S/CM

3.4.1(e)



0·2 S/CM

3.4.1(f)

(g) shows the effect of extremely high T_F, giving virtually zero frequency ripple with very slow synchronisation, low resonant frequency and persistent ringing. Note the long time scale of the oscillogram and the pronounced phase ringing ($f = d\phi/dt$).

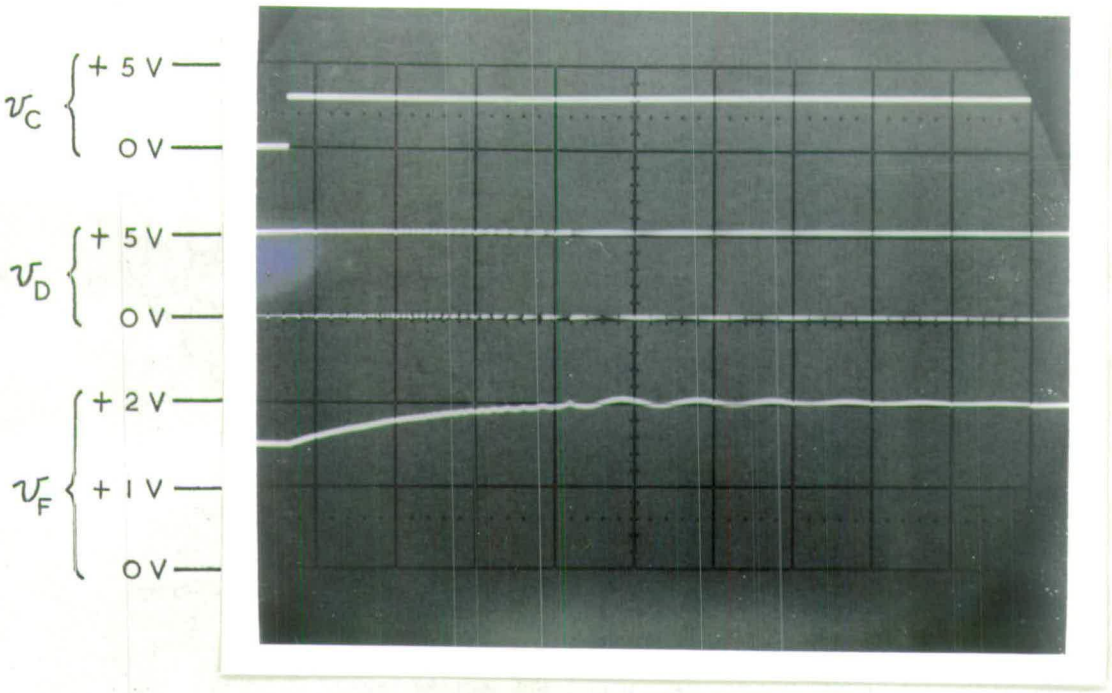
Oscillograms (f) and (g) show synchronisation by sudden change in direct control voltage v_c from zero to 3V; v_c is shown in the second trace. Initially a condition of false lock obtains, with pulse generator frequency below supply frequency. Sudden application of v_c within the pull-in range produces synchronisation followed by ringing (f) similar to that shown in (a). Smoothing which is adequate for 50 c/s operation is less suitable for the false lock shown in (f), and greatly increased smoothing produces the slow response shown in (g).

3.5 Internal Operation

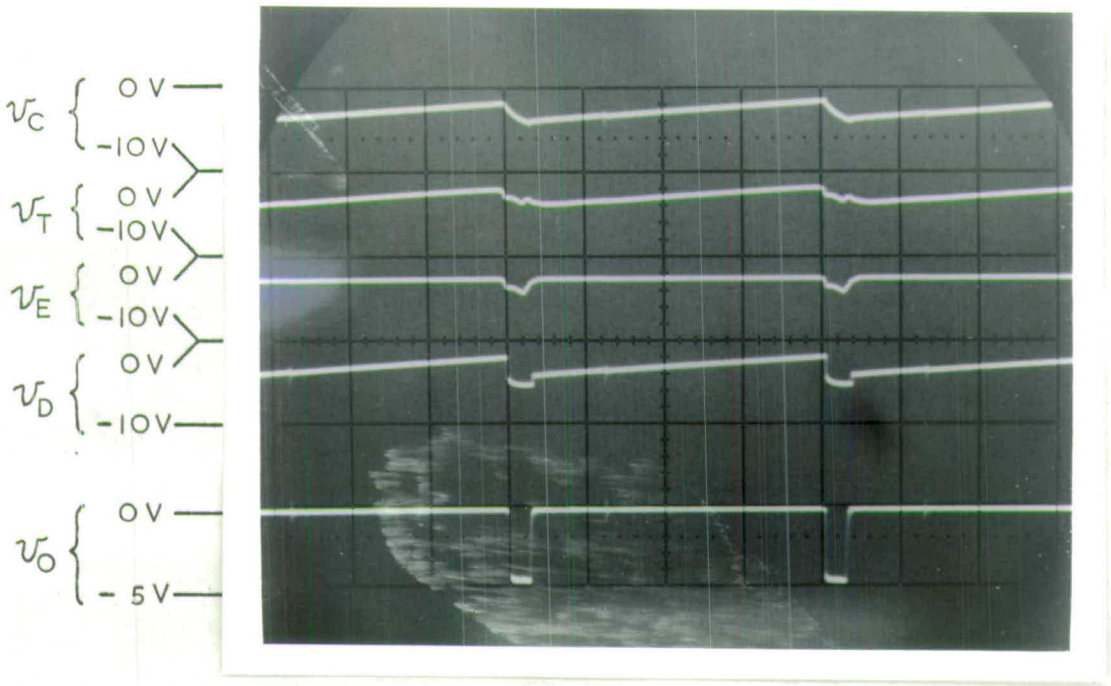
In this section oscillograms are used to illustrate operation of the principal pulse generator circuits.

3.5.1 Clock Pulse Generator

Fig.3.5.1 shows principal voltage waveforms. Top trace is capacitor voltage v_c, note linear rise followed by rapid exponential discharge. Second trace shows trigger input voltage v_t, showing equality to capacitor voltage until the trigger begins to conduct, then near equality to trigger common emitter voltage until the end of the discharge period. Third trace shows the emitter voltage v_e of the Schmitt trigger transistors: this shows a step change as capacitor voltage reaches trigger limits.

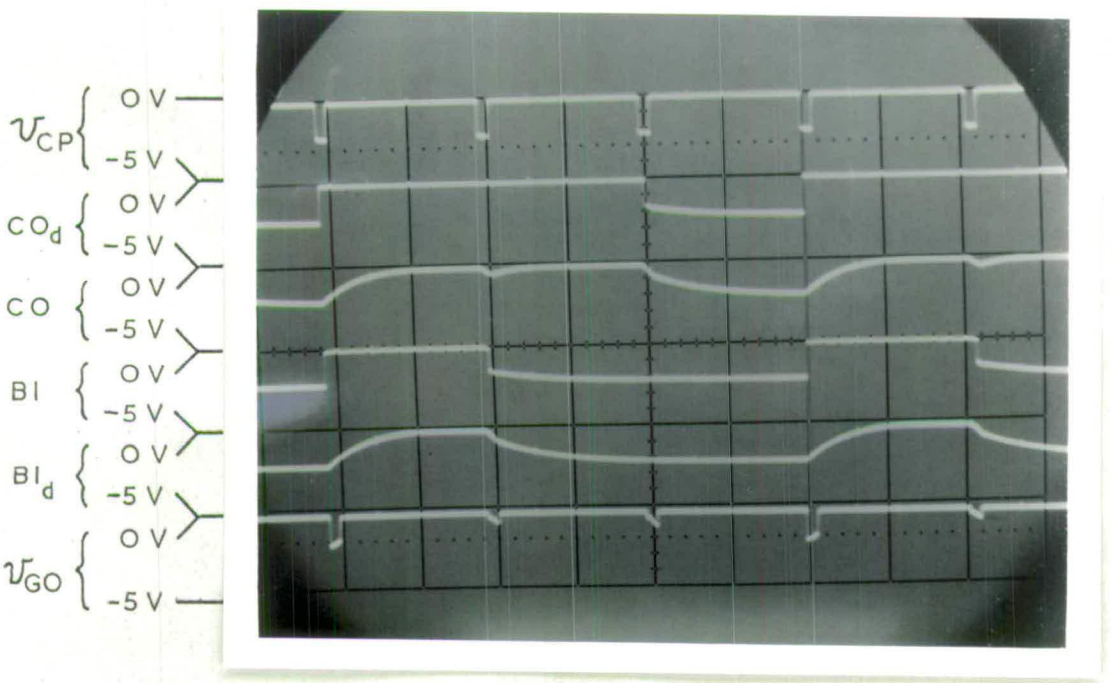


3.4.1(g)



10 μs/CM

3.5.1



20 μs/CM

3.5.2

Fourth trace shows voltage v_d at collector of capacitor discharge transistor; this equals capacitor voltage during the charging period, then is held negative when the transistor is turned on to discharge the capacitor. Fifth trace shows output voltage v_o of the unit; this is a digital indication of the state of the trigger. In this case, the output is loaded by other pulse generator units, so that the amplitude of the digit is less than 6V.

3.5.2 Ring Counter

Fig. 3.5.2 illustrates operation of the pulse steering circuit. Trace 1 shows incoming clock pulses v_{cp}, traces 3 and 5 are delayed versions of C_o and B_1 respectively. These three signals constitute the input to a pulse steering gate; when all are negative, the gate output (v_{go}, trace 5) becomes negative also. When this occurs, current is fed to the base of the left hand side transistor of bistable B, turning it on, as shown by the positive steps of trace 6. Traces 2 and 4 show voltages at the left-hand output of bistable C and the right-hand output of bistable B; for pulse steering purposes, these are called C_o and B_1 respectively.

Partial transmission of nominally suppressed clock pulses is shown in trace 6 coincident with loading of the delay circuit which is apparent as a small negative pulse in trace 5. Bistable B (trace 4) is not affected by these reduced clock pulses.

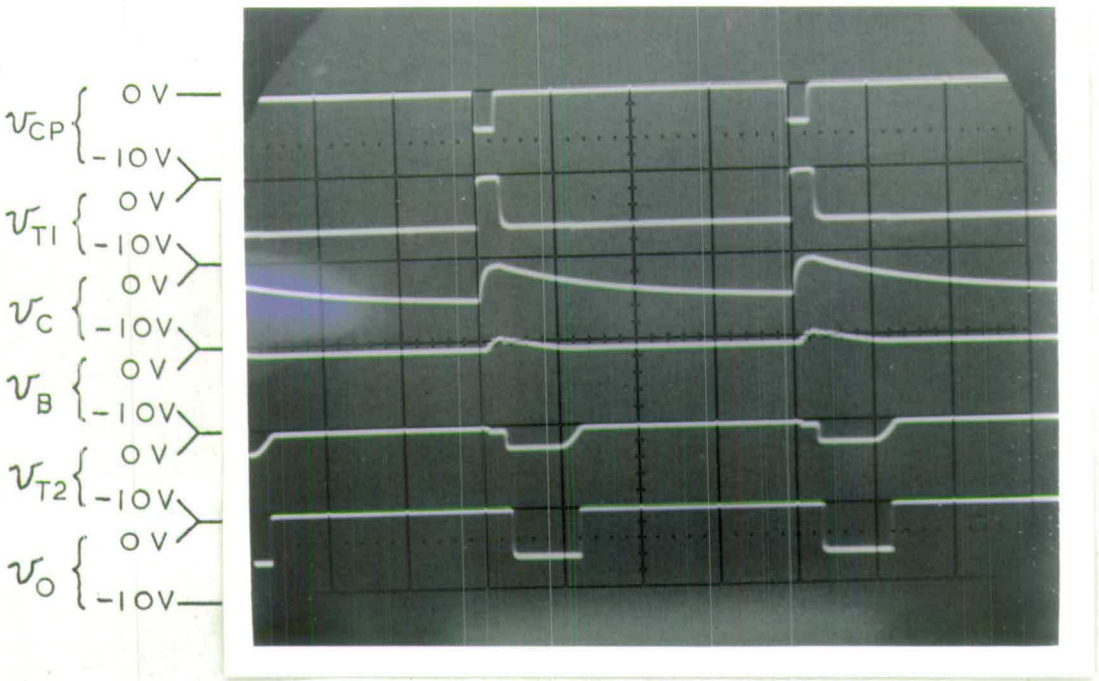
Redundancy of the input represented by trace 5 is apparent; this represents feedback from the output of a bistable to the input of the same bistable, and prevents indeterminate switching by the first clock pulse following application of the d.c. supply.

Ring counter output sequence is shown in traces 1 to 4 of Fig. 3.5.4(a); these represent voltages at the righthand side output of bistables A to D respectively; state "0" of each bistable is represented by negative voltage for decoding purposes.

Exponential decay from a small initial negative voltage toward a more negative value is caused by the capacitive load formed by the pulse steering circuit. The voltage steps at bistable state changes straddle the output logic level of $-1\frac{1}{2}V$ with only a small margin at either side, showing that pulse steering load is high, corresponding to design for high speed rather than for immunity from high noise voltage. In this case, maximum output speed has been raised from 670c/s to 4kc/s by substitution of $R_1 = R_2 = 4.7k$, $R_3 = R_8 = 1k$, $R_4 = R_5 = 2.2k$ in Fig. 2.3 and $R = 1k$ in Fig. 2.3.2(a).

3.5.3 Short Pulse Timer

Fig. 3.5.3 illustrates operation of this unit. Trace 1 shows clock pulses v_{cp}, second trace shows inverted clock pulses v_{t1} at the collector of transistor 1. Trace 3 shows capacitor voltage v_c; this is rapidly clamped nearly to OV during each clock pulse and charges negatively between clock pulses. Trace 4 shows voltage v_b at the base of the second transistor; this is proportional to v_c when the base is reverse biased. Trace 5 shows voltage v_{t2} at collector of the second transistor. During clock pulses this is held at OV less the forward voltage drop of one diode; a period of negative voltage follows, terminated when the second transistor receives base current from the capacitor circuit.



10μs/CM

3.5.3

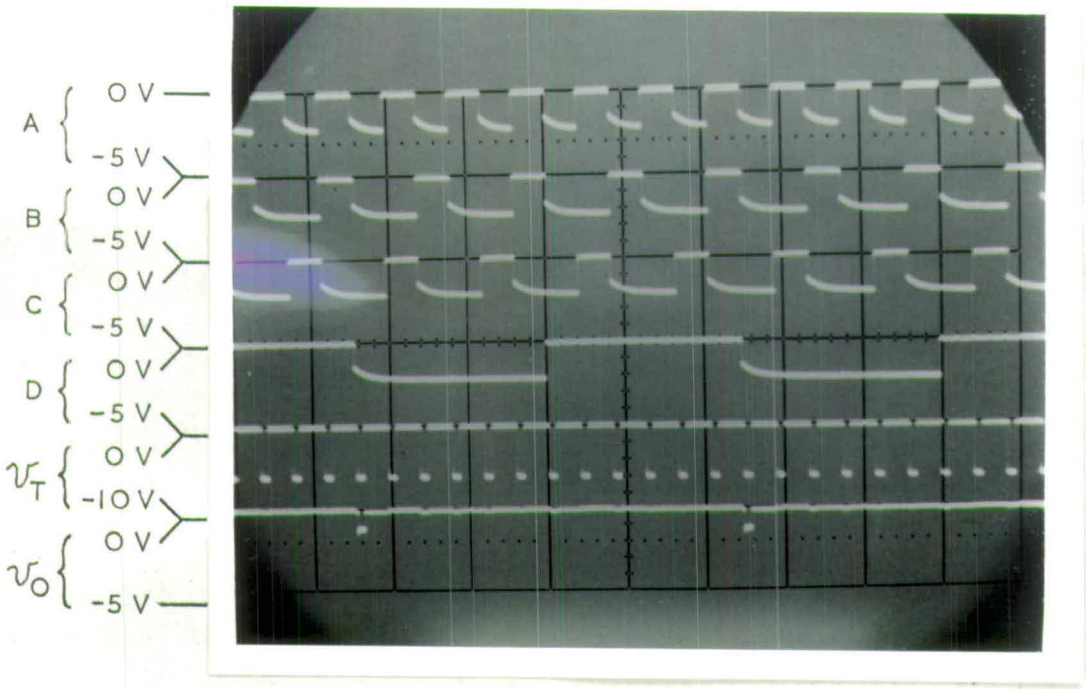
The output voltage v_o is a squared version of v_{t2}, trace 6.

3.5.4 Short Pulse Generator

The function of this unit is to decode a complex input signal and to amplify and isolate the decoded signal.

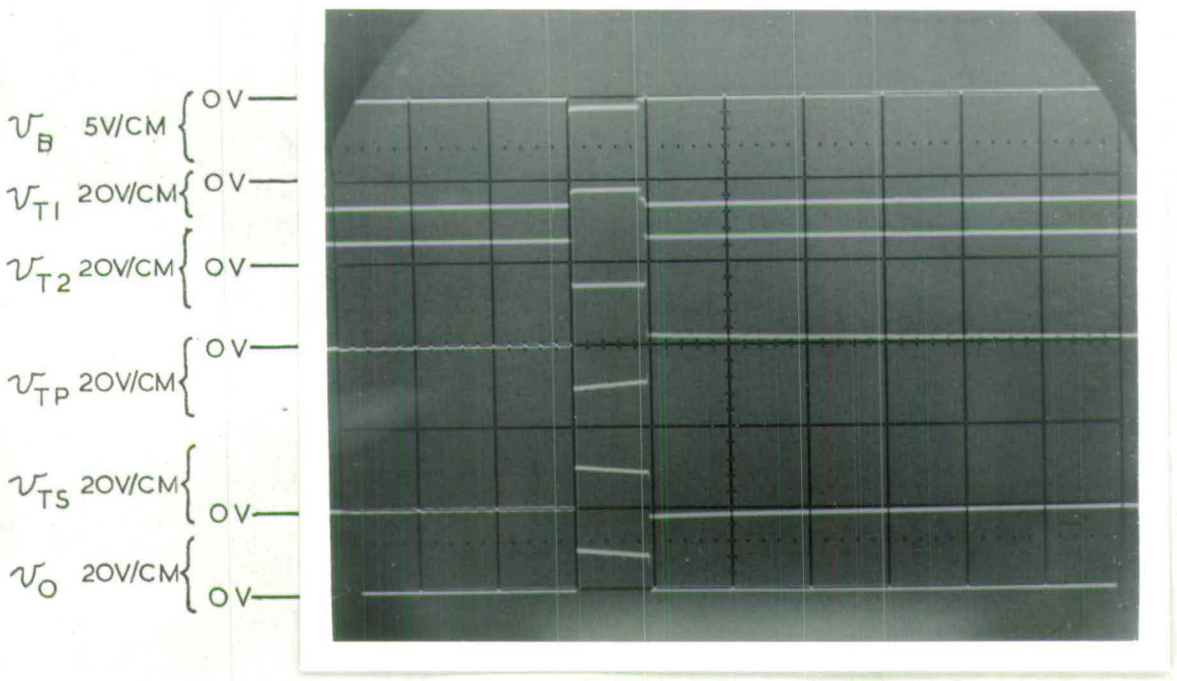
Decoding of the input signal is illustrated by Fig.3.5.4(a); traces 1 to 4 show signals received from the ring counter bistables, and trace 5 is the signal received from the short pulse timer. When all are negative, the decoding AND gate has negative output, shown in trace 6.

Fig. 3.5.4(b) illustrates amplification and isolation; top trace shows voltage v_b at the output from the decoding gate; the base of the first transistor T_1 is connected to this. Trace 2 shows voltage v_t, at T_1 collector, showing inversion of the input signal; third trace shows voltage v_{t2} at the collector of the second transistor T_2, showing another stage of inversion. This latter digit has 11V amplitude and is followed by a period with about 0.6V with opposite polarity to the 11V digit. Fourth trace v_{tp} shows voltage across the isolating transformer primary; this has nearly 11V initial amplitude, falling slightly towards the end of the pulse. At pulse termination, transformer primary voltage reverses, then decays almost exponentially; when 0.6V is reached, decay becomes very rapid; this is due to the magnetising current flowing through a resistor and diode in series, the diode giving the increased decay rate at low current by virtue of its increasing forward resistance with decreasing current. Fifth trace shows secondary voltage v_{ts}, this is similar to primary voltage illustrating



100μs/CM

3.5.4(a)



10μs/CM

3.5.4(b)

good transformer bandwidth; sixth (bottom) trace shows output voltage v_o; this is v_{ts} rectified, showing positive output only, plus a short negative spike caused by finite reverse recovery time of the rectifier.

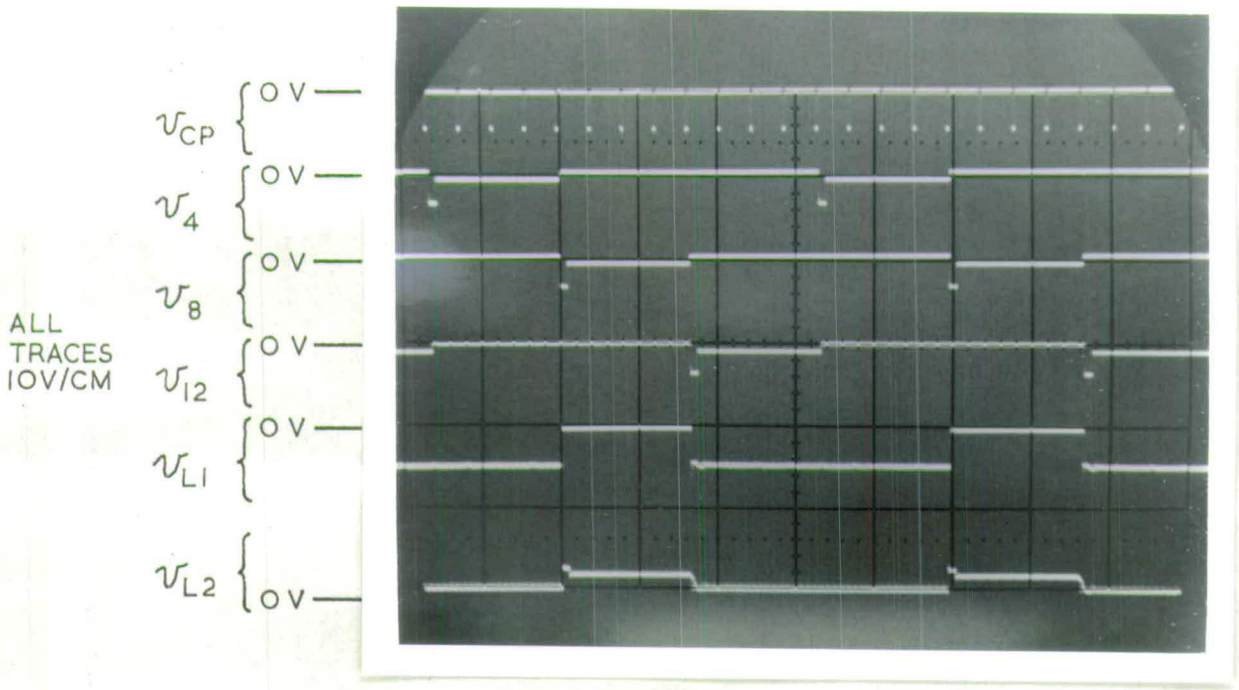
3.5.5 Long Pulse Generator

On/off control of long pulses is illustrated by Fig.3.5.5(a). Trace 1 shows clock pulses v_{cp}, traces 2, 3 and 4 show voltages at the "start" input and both "stop" inputs of one long pulse controlling bistable, showing the occurrence of control digits at intervals of 4 clock periods. Trace 5 shows bistable output $v_{\ell 1}$, showing initiation of a long pulse in response to a digit v_8 at the "start" input terminal, and termination in response to a digit v_{12} at one of the "stop" inputs.

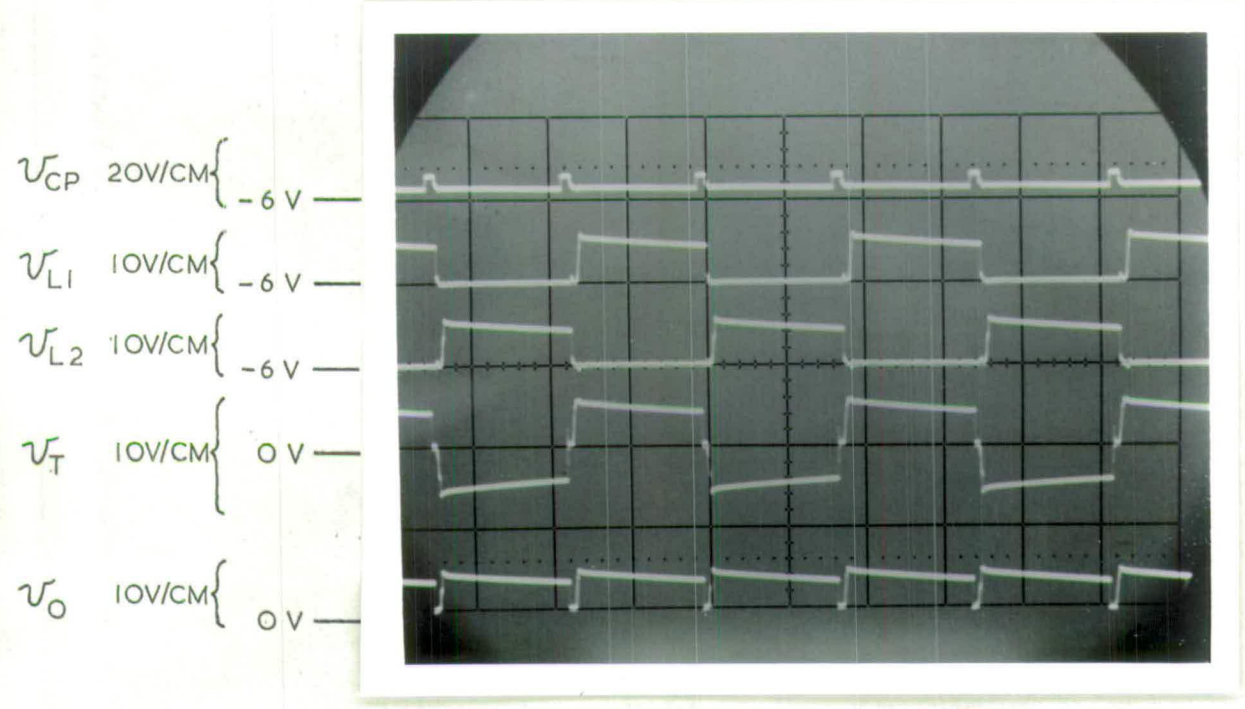
Trace 6 shows the long pulse $v_{\ell 2}$ after isolation, showing slight reduction in magnitude and gaps of short duration incurred in the isolation process.

Isolation of the long pulses is illustrated by Figs. 3.5.5(b), (c) and (d). In (b), trace 1 shows inversion switch clock pulses; these switch the bistable circuit which controls the clamping action of the inversion switch. Traces 2 and 3 show the voltage of lines L_1 and L_2 which are alternately held at -6V. Trace 4 shows transformer secondary voltage v_t of a long pulse generator, illustrating polarity reversal in unison with inversion switch changes. Trace 5 shows output voltage v_o of the long pulse generator, this is a full wave rectified version of v_t.

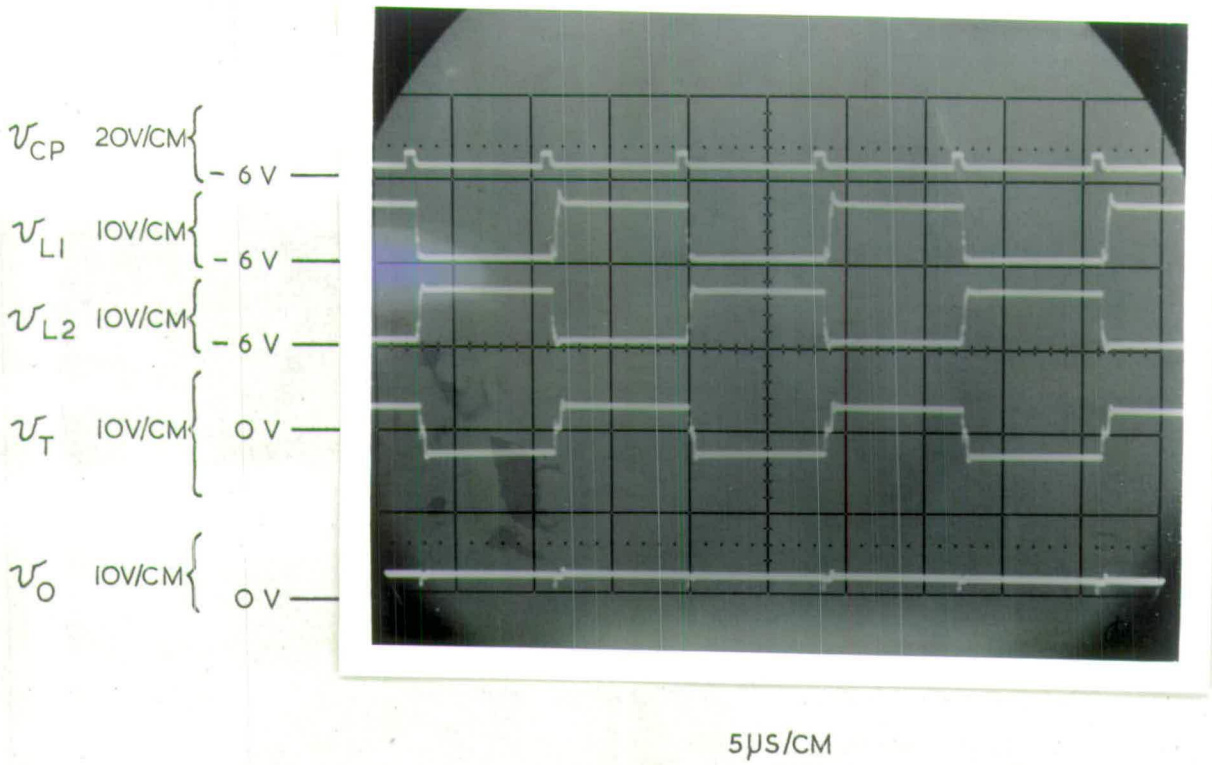
In (b) inversion frequency is low, showing pronounced decay of output voltage during each half cycle of inversion, caused by transformer magnetisation; load is 220Ω resistive.


v_{CP} 0 V
v_4 0 V
v_8 0 V
v_{12} 0 V
v_{L1} 0 V
v_{L2} 0 V
ALL TRACES 10V/CM
100μs/CM

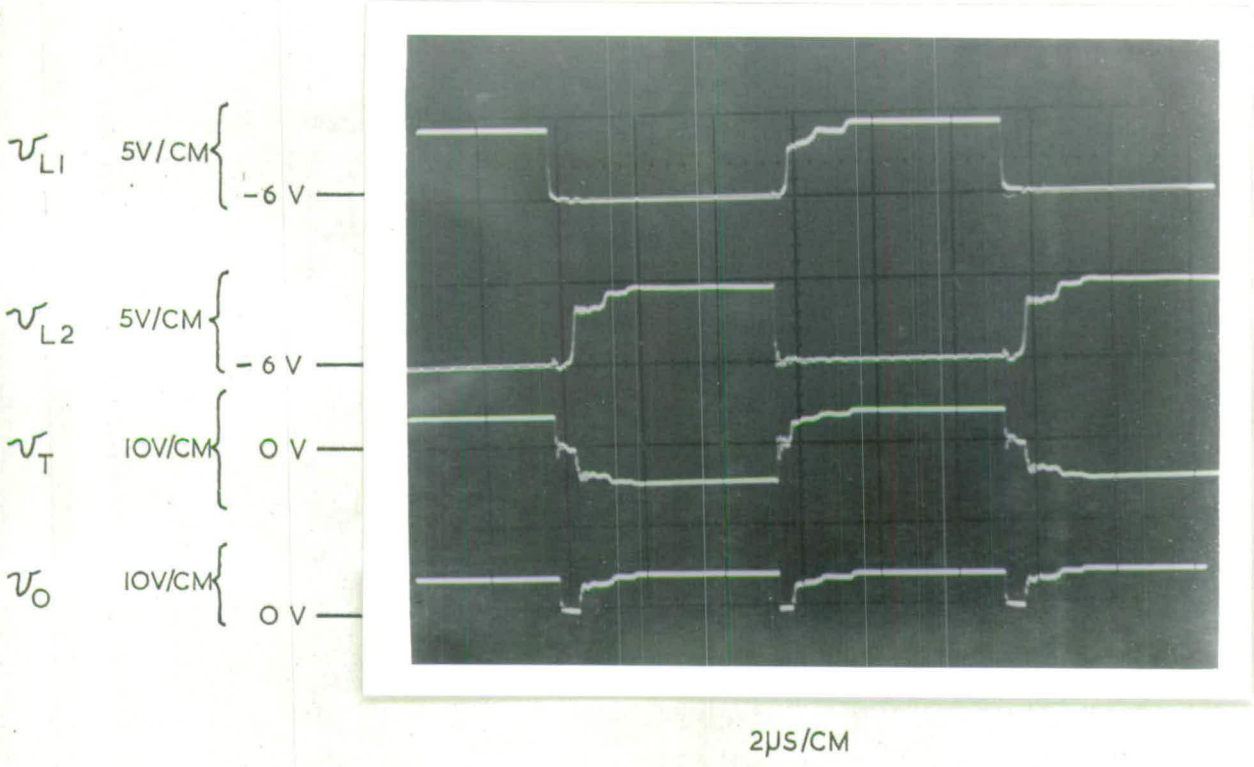
3.5.5(a)


v_{CP} 20V/CM -6 V
v_{L1} 10V/CM -6 V
v_{L2} 10V/CM -6 V
v_T 10V/CM 0 V
v_O 10V/CM 0 V
5μs/CM

3.5.5(b)


v_{CP} 20V/CM
- 6 V
v_{L1} 10V/CM
- 6 V
v_{L2} 10V/CM
- 6 V
v_T 10V/CM
0 V
v_O 10V/CM
0 V
5μs/CM

3.5.5(c)


v_{L1} 5V/CM
-6 V
v_{L2} 5V/CM
- 6 V
v_T 10V/CM
0 V
v_O 10V/CM
0 V
2μs/CM

3.5.5(d)

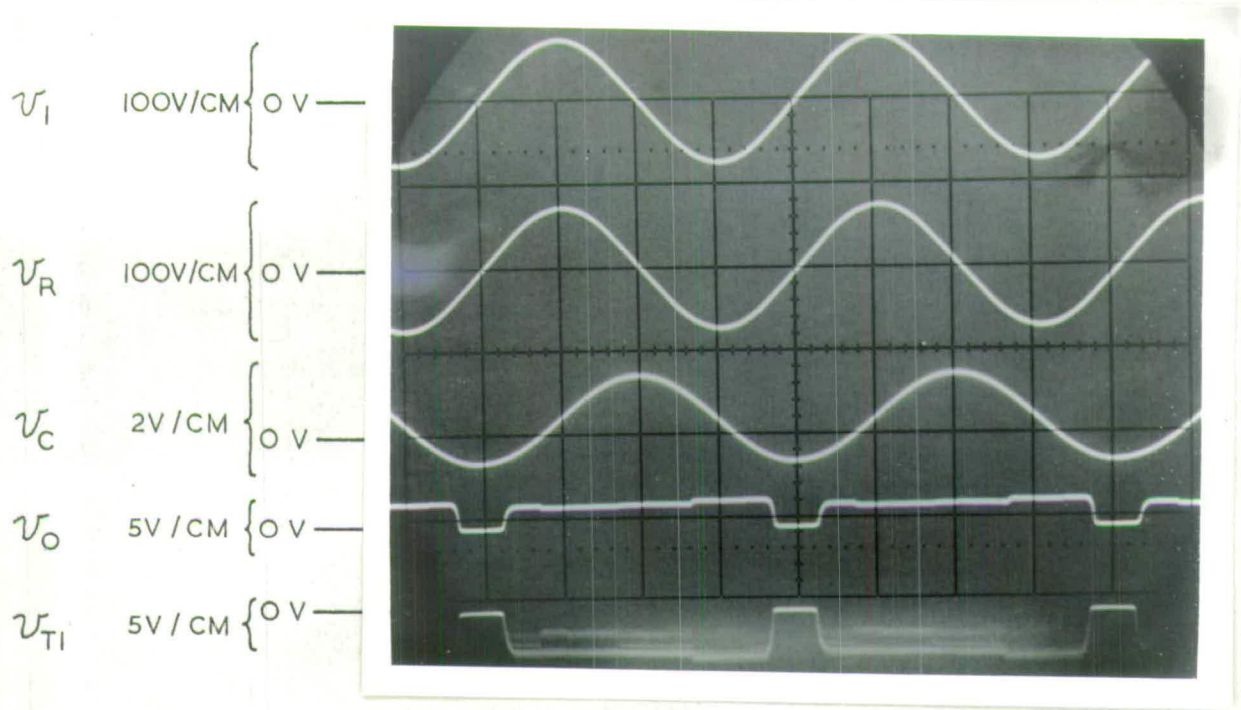
In (c), the load is two silicon p-n junctions in series; this is the control input of the transistor analogue inverter discussed in chapter 4. The v-i characteristic of the junctions maintains the voltage approximately constant throughout each half cycle of inversion, and charge storage in the p-n junctions maintains the voltage during gaps between blocks of inverted power.

In (d), the frequency has been raised to reduce the droop which occurs during each half cycle of inversion. Load is 220Ω resistive, and the gaps between blocks now occupy a greater part of each cycle.

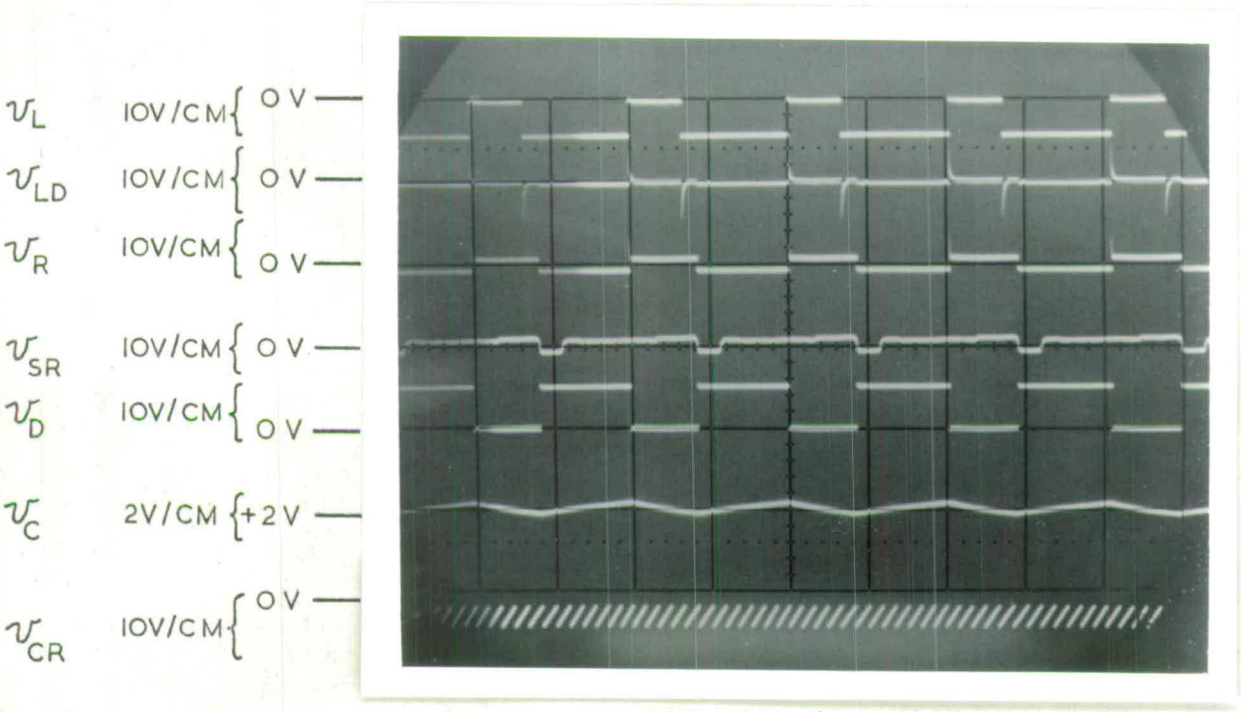
3.5.6 Phase Control

Fig. 3.5.6(a) illustrates derivation of pulses from the supply reference source. Trace 1 shows supply voltage v_1, second trace shows voltage v_R across R_1 (section 2.6.2) showing no great change of form incurred by the d.c. blocking stage. Trace 3 shows voltage v_c across the filter capacitor; reduction of magnitude and nearly 90^o lag are apparent, with d.c. offset caused by clamping the integral to $\angle$ + 0.6V. Trace 4 shows transistor collector-emitter voltage v_{t1} which becomes zero once per supply cycle as the integrated supply voltage is clamped by conduction of the transistor base. Trace 5 shows the pulse after isolation, diminished in amplitude.

Fig. 3.5.6(b) shows derivation of reference pulses from the pulse generator (section 2.6.1) and use of these together with supply reference pulses in the phase detector.


v_I 100V/CM 0 V
v_R 100V/CM 0 V
v_C 2V/CM 0 V
v_O 5V/CM 0 V
v_{TI} 5V/CM 0 V
5MS/CM

3.5.6(a)


v_L 10V/CM 0 V
v_{LD} 10V/CM 0 V
v_R 10V/CM 0 V
v_{SR} 10V/CM 0 V
v_D 10V/CM 0 V
v_C 2V/CM +2 V
v_{CR} 10V/CM 0 V
10MS/CM

3.5.6(b)

Top trace shows voltage waveform v_ℓ of a long output pulse before isolation; this is a suitable phase detector reference source. Second trace $v_{\ell d}$ shows the same differentiated (section 2.6.1) and third trace v_r shows the differentiated pulse after rectification, the resulting short pulse being ideally suited to control of the phase detector. Fourth trace v_{sr} shows pulses derived from the supply reference, and fifth trace shows phase detector output voltage v_d; this illustrates switching of the bistable phase detector into one state by supply reference pulses, and into the other by pulse generator derived pulses. Increasing lag of pulse generator relative to supply increases the mean positive value of phase detector output, in turn raising pulse generator frequency. Sixth trace shows filter capacitor voltage v_c, showing the triangular waveform produced by integration of phase detector digits, and seventh trace shows the clock pulse generator ramp waveform v_{cr}, showing frequency fluctuation in unison with v_c. For this illustration, filter capacitor size was reduced to give exaggerated frequency fluctuation, but this is nevertheless difficult to detect from the bottom trace.

CHAPTER 4

APPLICATION

In this chapter applications are described which illustrate use of the pulse generator in different control modes, and use for transistor inverter control as well as for thyristor control.

4.1 Thyristor Control

The pulse generator was used to control thyristor inverters in both the frequency controlled mode and synchronously with the a.c. supply in the phase controlled mode.

Automatic frequency control is illustrated by the honours project of Mr. C. Pratt, in which tachometer feedback was used together with an input reference signal to control pulse generator frequency. The inverter fed an induction machine at this frequency, closed loop speed control was thereby achieved. A filter network was used to couple reference and tachometer signals to pulse generator input to control transient response.

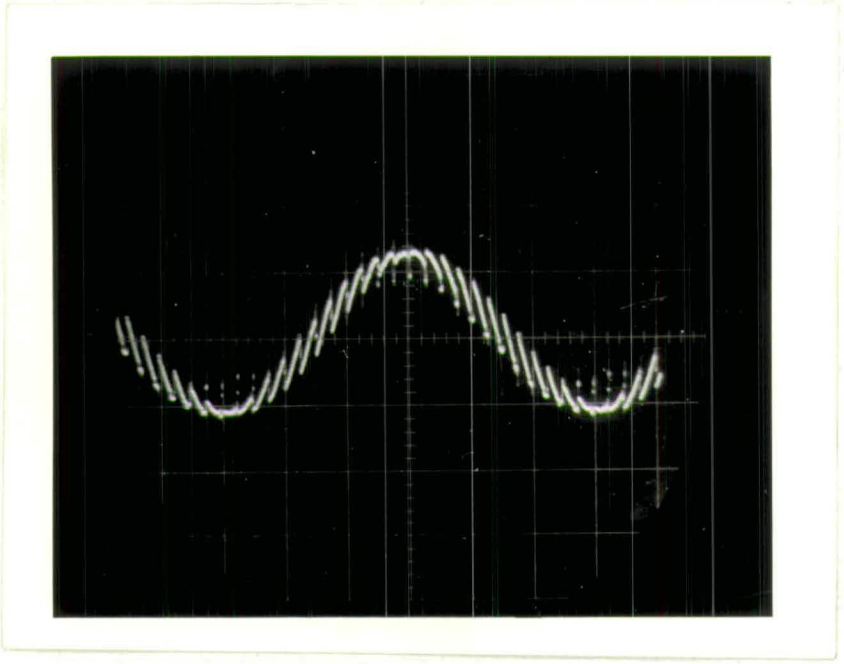
Phase control is illustrated by the honours project of Mr. R. Auchinleck. The inverter in this case was coupled to the a.c. supply and run synchronously with the supply. The primary objective of reversible rectifier operation was achieved, with direct current flow in either direction at constant direct voltage; in addition, disconnection of feedback diodes allowed operation as a force-commutated controlled rectifier, and a form of cycloconversion was obtained with asynchronous running. Force-commutated controlled rectifier operation was tested with continuous direct current over

the full 360° range of phase control. The direct voltage was plotted against phase difference and a sinusoidal characteristic obtained. Cycloconversion was also performed with continuous unidirectional output current, and represented operation as a force-commutated controlled rectifier with firing angle delay continuously changing at a uniform rate. Connection of the phase control circuit gave operation with supply and pulse generator frequencies related, operation with phase control disconnected gave unrelated frequencies. Fig. 4.1 shows output voltage with frequency ratios of 3:4 at (a) and 4:5 at (b); in each case, pulse generator frequency was below supply frequency.

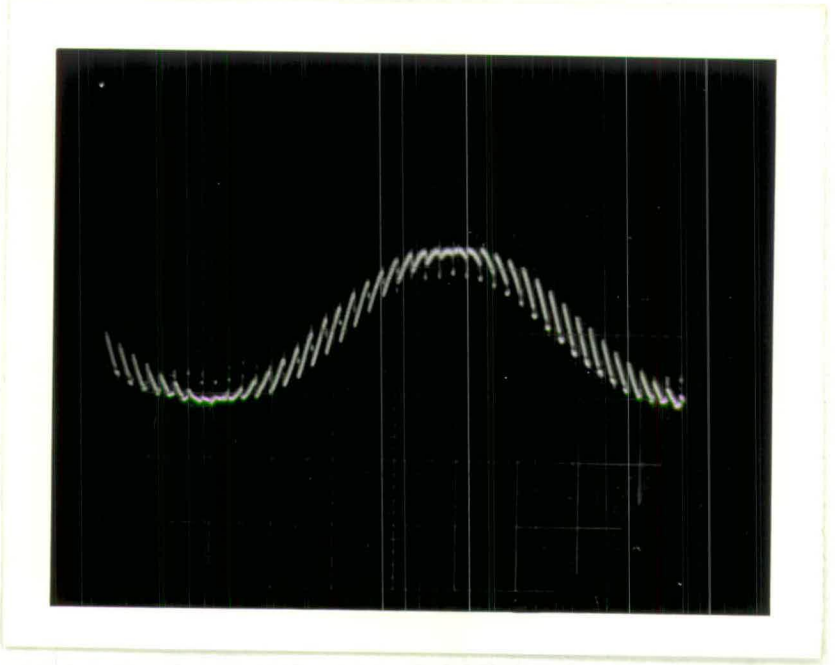
4.2 Transistor Control

Detailed analysis of parallel coupled thyristor inverter groups is complicated by the presence of commutation circuits and by the finite turn-off times of the thyristors; a transistor inverter having the same basic configuration is much simpler to analyse.

The long pulse outputs from the pulse generator are ideally suited to the control of transistors; accordingly, a transistor inverter was used as an analogue of the thyristor inverter, to facilitate investigation into the operation of some inverter circuits.



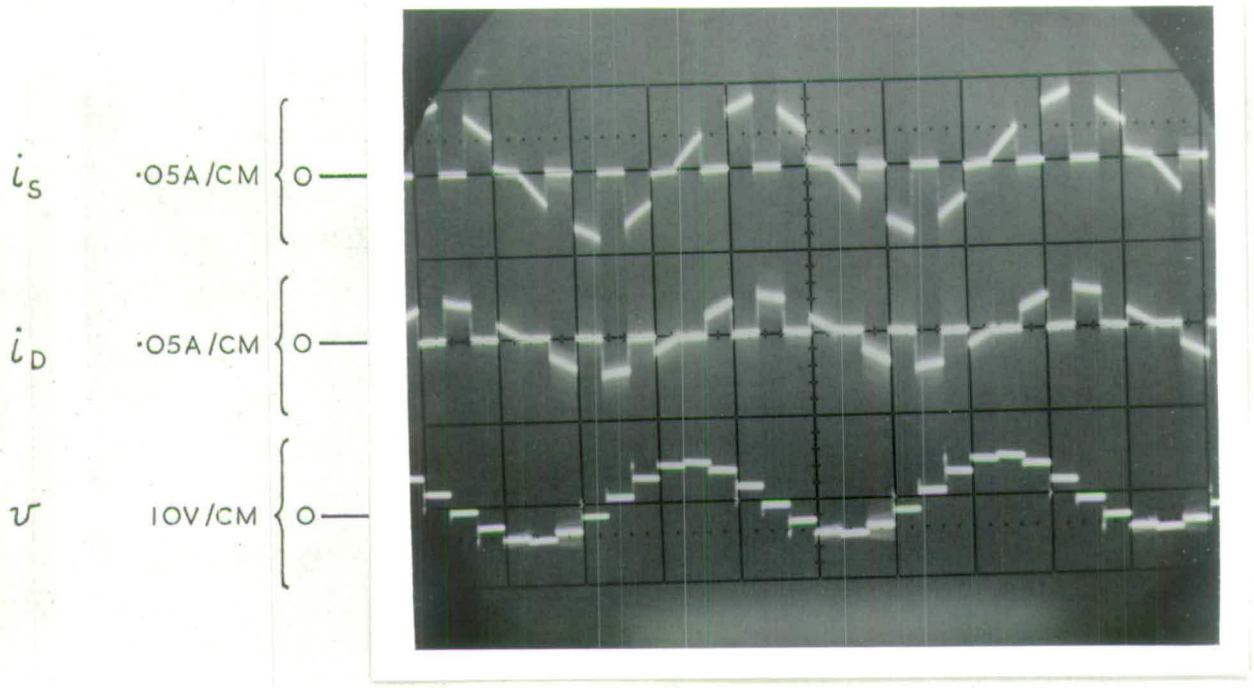
4.1(a)



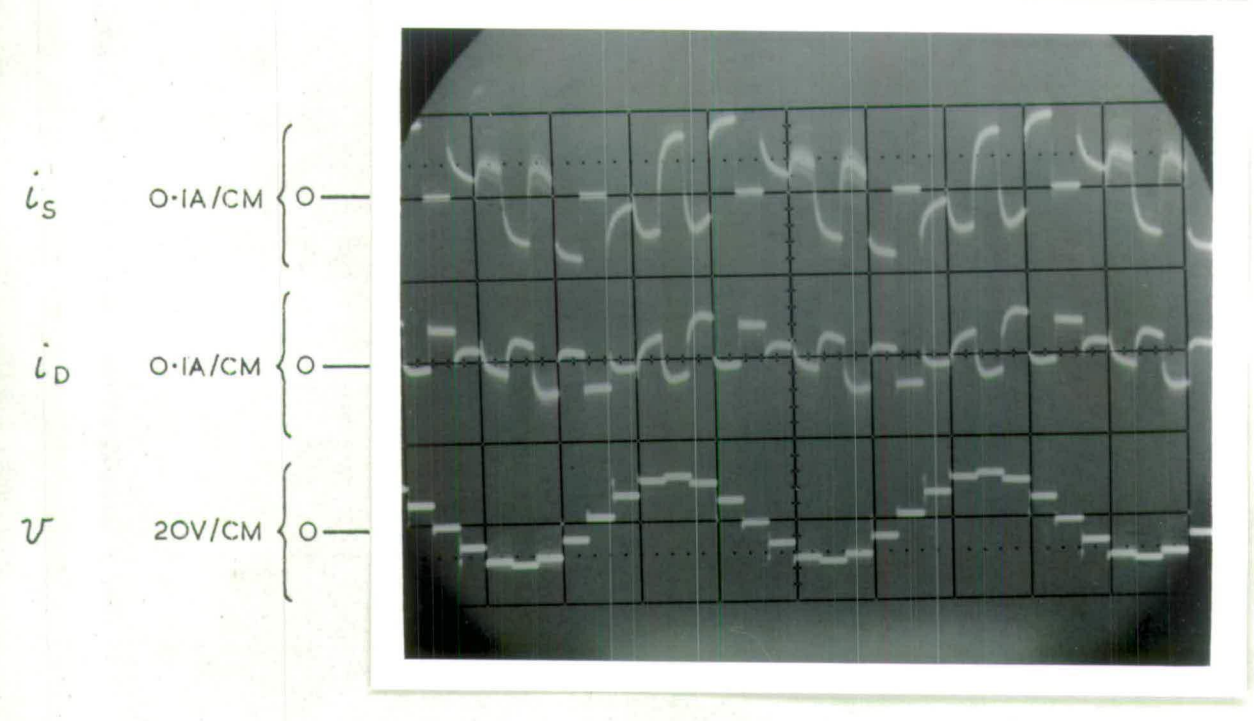
4.1(b)

Use of the transistor analogue technique is exemplified by the oscillograms of Fig.4.2, in which coil voltages and currents are shown for a 3-phase transformer coupled to a double 3-phase bridge inverter, with ring-of-3 operation. The inverter used transistors as active elements to simplify operation in respect of switching speeds, and no balance circuit was used, to facilitate investigation into interference between the two 3-phase bridge inverters. The inverters were coupled to a common fixed-voltage d.c. supply, and to star and delta windings on the transformer, to give correct phasing of the fundamental wave from each inverter group, with 6-phase overall operation.

In (a), the d.c. supply voltage is low, so that semiconductor forward voltage drops exceed the discrepancy of e.m.fs. induced in the windings by the two inverter groups; the main magnetising current is seen to chop from one inverter group to the other at each clock pulse. Top trace shows current i_s in one coil of the star connected transformer primary, trace 2 shows current i_d in the delta connected coil on the same limb. The total ampere turns can be seen to have approximately sinusoidal form, since this quantity is proportional to $i_s + i_d\,3$ and the amplitude of i_s is about 3 times the amplitude of i_d. While current flows in one coil the current in the other is zero. Trace 3 shows the voltage across an unloaded coil on the same limb, showing the stepped waveform characteristic of voltage-forcing inversion.


i_S
·05A/CM
O
i_D
·05A/CM
O
v
10V/CM
O
5MS/CM

4.2(a)

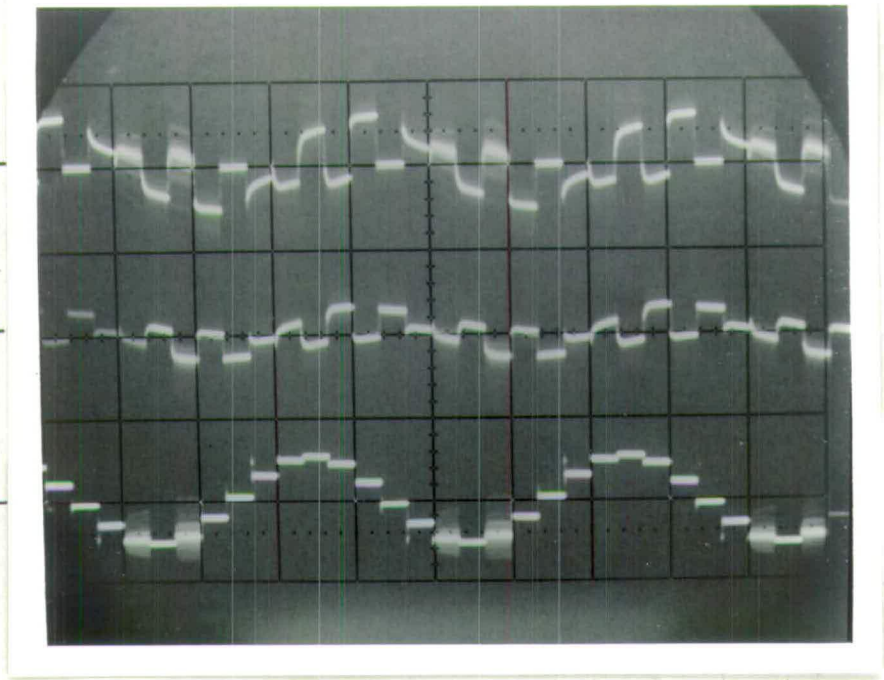

i_S
0·1A/CM
O
i_D
0·1A/CM
O
v
20V/CM
O
5MS/CM

4.2(b)

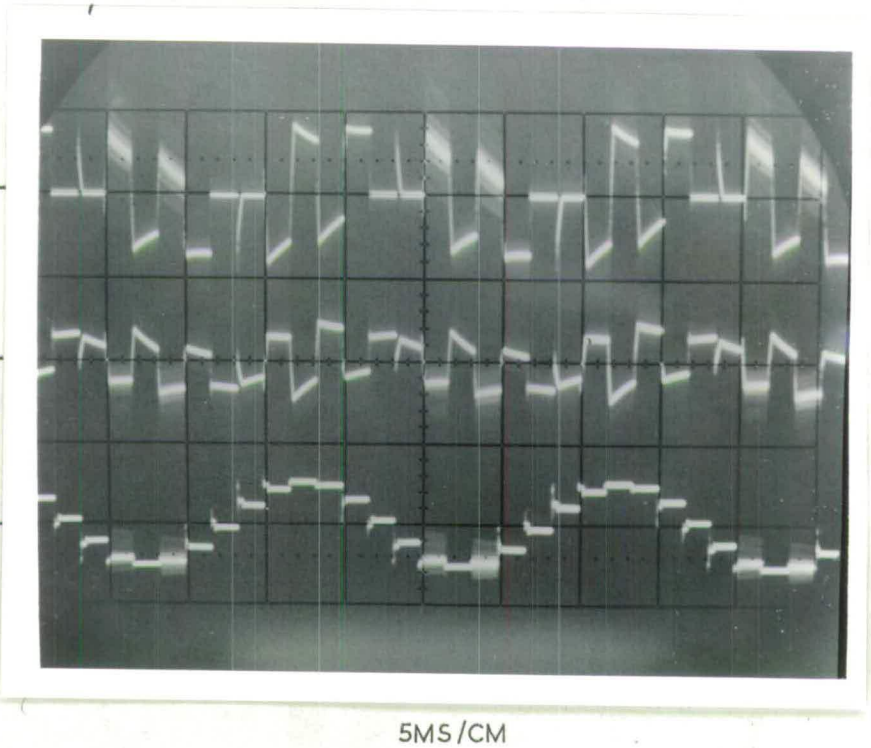
In (b), the supply voltage has been raised to produce positive interference between the inverter groups; current reversals replace the current zeros of the previous case, and the coil currents are seen to chop between two sinusoidal waves, indicating the presence of a sinusoidal e.m.f. difference between the two inverter groups. In addition, the individual current blocks have departed from the trapezoidal shape of the previous case, indicating the presence of continuously varying circulating currents superimposed on the basic sine wave-to-sine wave chopping.

In (c), the operating frequency has been reduced. The waveform of the transient following each chop is the same in both (b) and (c); in the latter, cycle time is longer and the overall effect of the transient on the sine wave-to-sine wave chopping is reduced. This shows that the waveform of the transient is dependent on circuit impedance rather than on the frequency of the forcing function. In the "interference" condition, a path exists for power flow between the inverter groups at virtually zero impedance, therefore the circulating current may have slowly varying components such as the transients recorded here.

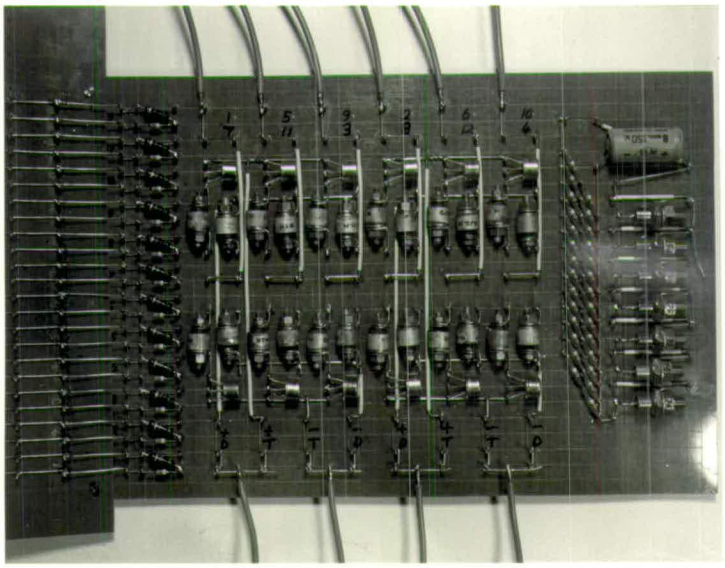
In (d) the supply voltage has been increased still further so that the circulating current far exceeds the transformer core magnetising current; reversion to trapezoidal waveform is apparent, indicating simplicity of the circulating current waveform throughout each clock period (one clock period = 1/12 inversion cycle); in this condition, resistance and inductance are the dominant impedances. At lower voltages, circuit resistance and inductance have less effect.


i_S 0·2A/CM
i_D 0·2A/CM
v 20V/CM
10MS/CM

4.2(c)


i_S 0·2A/CM
i_D 0·2A/CM
v 50V/CM
5MS/CM

4.2(d)



THE TRANSISTOR INVERTER

4.2(e)

CHAPTER 5

COMMENTS

In this chapter the design of the pulse generator is discussed and suggestions made for its improvement and adaptation for various purposes.

5.1 Circuit Design

In chapter 1 the requirements are shown to be met by circuits in which 3-layer transistors are used to produce pulses by rapid switching of a supply which is constant or practically so.

Basic power supply voltage (12V) was chosen to suit as many sources as possible; these include primary and secondary batteries and stabilised voltage supplies. Integrated circuits usually require a lower supply voltage than 12V, therefore these may be incorporated if necessary and supplied via a voltage dividing circuit.

A small number of discrete component types were chosen, having characteristics suitable for the use envisaged. Circuits were designed to use these standard components, to achieve as nearly as possible ideal operation in respect of overall input, transfer and output characteristics.

Transfer (control) characteristics have been given wide range; for example frequency range is very wide, so that exploratory trials can be made over the full range of useful inversion frequency and phase. Ranges may easily be reduced to suit special requirements, giving improvement in other directions.

Output voltage and current levels were chosen to suit the standard components; special requirements may be met by suitable alteration.

5.2 Use of Transistors

Most of the transistors are used in the common-emitter mode, to give voltage and current amplification; and have emitter terminals connected to the common supply. Operation in the saturated switching mode gives standard digits, related to and limited by supply voltages.

Current amplification enables logic to be performed at low power, controlling high output power from a common supply voltage. Voltage amplification enables losses due to forward voltage drops across diodes and resistors to be accepted, together with a noise margin, between stages of amplification.

Saturation ensures squaring of the output and immunity from small effects at the input; such as drift with temperature of diode forward voltage drops. Saturation is assured in the "on" condition when base current exceeds collector current divided by static current gain; that is, $i_b > i_c/h_{FE}$. Zero conduction (neglecting leakage) is given by zero or reverse base bias.

5.3 PNP versus NPN logic

NPN transistors represent better value than PNP transistors for a given switching speed, in terms of maximum rated collector voltage and current.

NPN transistors are used in the production of short output pulses, to fire thyristors. The small current rating of high speed germanium diodes determined current levels at the ring

counter decoding matrix; the number of stages of amplification required between ring counter and short pulse output determined the polarity of the ring counter logic, this uses PNP transistors.

In the production and isolation of long output pulses, each inversion switch transistor conducts the sum of the currents from several long pulse generators, therefore the former transistors are NPN and the long pulse generators use PNP transistors.

5.4 Switching Speeds

In most of the circuits switching speeds are not critical, for example use of the short pulse timer to hold off all outputs during clock pulses renders consideration of ring counter transient states unnecessary.

Short output pulse rise time must be short to ensure satisfactory thyristor operation; rapid switching of transistors in the short pulse generators is assured by the rapid build-up of large base currents. Output pulse fall time is not critical so no arrangement has been made for rapid transistor turn-off. Simple resistive coupling circuits without "speed-up" capacitors give the desired effect. The decoding gate controlling each short pulse generator feeds a transistor base directly, giving current transfer at virtually constant voltage; this constitutes a "squaring" circuit, giving both rapid rise and rapid fall to the short output pulse; the following amplifier stages accentuate the rapid rise at the expense of fall time.

The long reverse recovery time of diodes which have adequate current rating for long pulse isolation renders slow switching

inevitable during inversion switch commutations with the present circuit. This gives rise to gaps in the isolated long pulse waveform.

5.5 Isolation

The method of isolation used for short pulse outputs places a limit on output pulse duration. The use of short pulses is limited to firing thyristors and holding thyristors on for short periods only; the latter may be a requirement in an inverter operating at high frequency, or with short thyristor "on" periods.

The use of a high frequency carrier system to isolate long output pulses renders maximum pulse duration independent of transformer size.

The present long pulse is not ideally suited to thyristor firing as the gaps in the isolated waveform give rise to marginal firing when these appear during the firing period; this effect may be reduced by reduction in switching times of the isolation circuit or eliminated by use of a multiphase carrier system rather than a single phase system.

Long pulse termination is complicated by transformer magnetisation, this gives exponential decay. Energy fed to the load in this period depends on the part of the inversion cycle involved, lack of synchronism causing jitter.

The present long pulse isolation is performed by a single pair of transistors which alternately clamp the voltage levels of isolating transformer primary windings to $\pm$ 6V, less losses and less the voltage across the droop resistor; each transformer is

fed via diodes, so that there is no interaction between the outputs. The long pulse output is the rectified transformer secondary voltage. Provided that the rectified output current exceeds transformer magnetising current throughout each cycle, variations in magnetic energy content may be accommodated by variations in primary circuit current.

Droop resistors are placed in the primary circuit of all output transformers; this enables initial s/c output current to be equal to the maximum rating of the relevant switching transistor.

5.6 Frequency Control

Requirements may arise for control of inversion frequency from zero to several kilocycles, for example in the speed control of a machine with good power to weight ratio. Control of an induction machine down to zero speed with overhauling load demands reversal of inversion frequency, and in some cases continuous control in one range from positive to negative frequencies may be required.

5.6.1 Clock Pulse Generator

The clock pulse generator is a Schmitt trigger oscillator in which capacitor charging current is almost perfectly proportional to an input signal; capacitor discharge is virtually instantaneous, so that output pulse frequency is proportional to control signal amplitude. This is a simple circuit with only one timing element, and the output may easily be arranged to have either polarity and any required magnitude.

Errors causing departure from proportionality of the control current v. frequency characteristic arise because current is diverted from the capacitor charging circuit into various paths:

1. input buffer.
2. capacitor internal leakage.
3. leakage into discharge transistor less reverse leakage from trigger.
4. trigger input current.

Losses to 1 depend on variation of h_{FE} with emitter current in the present single transistor buffer, and are a high proportion of input current when this is small, i.e. at low frequency. Losses to 2 and 3 are a constant small current drain, and 4 occurs only at the upper triggering point.

Variation in trigger input levels will cause the input current/output frequency rate to change; such variation will occur because of temperature change and operating frequency, the latter effect arising from the finite switching time of the transistors.

For the clock pulse generator to run, the input control current must exceed the losses 1 to 4 above; the upper frequency limit is set by output pulse duration and transistor switching speeds. As the input current rises to a value comparable with capacitor discharge current, the discharge time and therefore the clock pulse duration both increase. The upper frequency limit is therefore somewhat lower than (low frequency clock pulse duration)$^{-1}$.

The majority of applications of the unit will involve voltage control of frequency rather than current control because of the fixed supply voltage used in most complex control circuits. The greatest source of error in the control voltage v. frequency curve arises from the considerable input voltage (approximately 0.5V) of the clock pulse generator. No attempt has been made to

reduce the error by use of large control voltages, because the use of an improved input circuit may reduce the error by several orders of magnitude, whereas the former approach gives improvement in direct proportion to voltage only.

The requirement for continuous control of pulse generator frequency from positive to negative values may arise in machine control, for example in reversible drives and in control of induction motor speed down to zero with overhauling load. This requirement may be met by special switching systems controlling the ring counter forward-reverse switching sequence or by continuous analogue control of frequency through zero.

Frequency control by proportional d.c. analogue in one continuous range from positive to negative values of frequency may be achieved by the use of two clock pulse generators, with common input terminal. The pulse generators must have virtually perfect control characteristics; one pulse generator steps the ring counter forward, and the other steps the ring counter backward.

5.7 Ring Counter

The present ring counter is a coded binary type having outputs following a fixed sequence in response to input clock pulses. The state of the counter may be recognised at all times throughout the output cycle by reference to the output voltages. The binary coding used gives rise to simple circuitry.

Frequency division is accomplished in several stages; bistable A halves the input frequency, bistables B and C together divide the input frequency by 3. Bistables B and C have 4 possible

states of which 3 are used, this giving rise to redundancy of stable states and possible starting transients not included in the running rota.

Bistable A switches freely without guidance from other ring counter bistables; B and C are steered by each other and constitute a selfcontained tristable circuit; bistable D switches once per complete cycle of A, B and C combined, thus halving the output frequency of the ring of 6 formed by bistables A, B and C. This arrangement was found to give simpler pulse steering circuitry than would be required for other sequences; most of the complexity involved is in the pulse steering controlling bistable D, and this has been performed by simple circuitry by compounding the AND gates involved; considerable unison between the signals involved has made this possible.

The design philosophy has been to give each ring counter bistable circuit its own pulse steering feedback so that clock pulses cannot be applied to confirm an existing state; additional pulse steering circuitry is used to further restrain pulse application so as to achieve 2, 6 and 12-stable operation of the 4 bistable circuits.

The pulse steering circuits controlling one bistable in response to the output from another render some of the simple pulse steering feedback redundant in continuous running; the circuits have been retained to simplify starting transients, so that correct operation is achieved following application of the first clock pulse.

The pulse steering circuit constitutes the major lag in ring counter operation; the charging time of the "memory" capacitors determines the upper frequency limit, above which pulse steering is erratic. The time constant of the RC delay circuit is determined as follows: C must be adequate to conduct clock pulse current with total voltage change less than bistable logic input level; R must be of low resistance to minimise RC, but must not be so low as to affect bistable output logic.

Logic voltage levels of the circuits controlled by the ring counter have the greatest possible tolerance in the lower level (transistors "off"); this is the region in which loading by the pulse steering circuit affects output voltage, therefore the load tolerance is large and R (above) may have low value. Delay circuit loading imposes an a.c. load on bistable outputs, giving the curved lower part of the output voltage waveform, Figs.3.5.2 and 3.5.4(a). Output logic levels cross the trace above the curved portion.

The small voltage difference between logic levels at short pulse generator input minimises the effect of stray capacitance and gives current transfer almost as rapidly as current change at source; this squares ring counter output and short pulse timer output, giving short pulses with rapid rise.

Reduction in internal load resistance of the ring counter (R_3 and R_8; Fig.2.3) would enable heavier pulse steering loads to be supplied, so that maximum operating frequency could be raised. The component values given in section 3.5.2 give the maximum operating

speed for the given clock pulse duration and internal load; reduction of internal load resistance detracts from efficiency.

Clock pulse duration has been made long to facilitate ring counter switching with critical loads, giving good use of ring counter transistors. Higher frequencies would be obtained by the use of shorter clock pulses, for which pulse steering capacitance could be reduced.

5.8 Short Pulse Generation

The short pulse timer determines the duration of short output pulses, and its action prevents spurious outputs from being produced during switching transients of the ring counter.

A resistor-capacitor-transistor timing circuit is used, with rapid, positive resetting and diode-transistor logic to form the required output signal. A squaring circuit at the output eliminates the need for sensitive discrimination in the coupling from the capacitor timing circuit to the following digital stage, and this coupling is made adjustable to control the output pulse duration.

Short pulse generators produce pulses in response to the combined outputs of the ring counter and the short pulse timer; these signals are at low level, to suit the low cost, high speed diodes and the high efficiency required of the unit; the low level signals are decoded, amplified and isolated.

5.9 Circuit Simplification

The original design had short pulse outputs only; long pulse outputs are a later addition. Long pulse control and ring counter outputs are both digital, stepped by clock pulses; therefore a more economical system may have long pulse control and ring counter circuits combined.

The composite output pulse may be produced using long pulse generation only; a pulse shaping circuit could be used to transmit the pulse undiminished initially, with amplitude falling to a lower level to suit thyristor mean gate power rating.

In the case of the Honours projects of Mr. R. Auchinleck and Mr. C. Pratt, short pulse generation was omitted for simplicity. Long pulses were used for thyristor firing and holding; heavy currents were not used in the thyristor circuit, and no damage to thyristors was apparent.

Circuit complexity may be reduced by the use of 4-layer p-n-p-n devices to perform bistable functions instead of 3-layer devices; anode circuit turn-off time would be an operational complication in parallel commutated circuits, but small 3-terminal p-n-p-n devices are easily subjected to gate control.

Four tristable circuits driven by clock pulses are the minimum ring counter requirements forthe double 3-phase bridge inverter; outputs of suitable polarity may be coupled directly to long-pulse isolation circuits, and thence via linear pulse forming circuits to the thyristor gate terminals. This system is a low power four-rings-of-3 inverter used for gate control of a larger one. Alternately, a ring of 12 bistable circuits coupled via diode OR gates to long pulse isolation circuits give a simple system which may be programmed to suit different types of inverter.

5.10 Phase Control

Phase control consists of the control of the phase of one signal relative to another signal; in the pulse generator, relevant

signals are the reference (power supply voltage) and the output pulses.

In the phase control of thyristor inverters, gate signal pulses must be controlled in phase relative to the supply voltage reference. This may be brought about by a variety of methods, such as those outlined below:

1. open loop control
2. closed loop control
3. individual control of each output
4. common control of all outputs

All permutations of methods 1 and 2 with methods 3 and 4 are possible. 1 gives simple operation, 2 (phaselock) may be used to give special operation, such as continuous pulse generation in the event of supply reference failure, and control of a multiphase pulse generator using a single phase supply reference. The local timebase inherent in phaselock loops gives operation in the frequency controlled mode if required, without additional circuitry.

3 may be used to give special operation in the event of power supply phase failure, or lack of balance in the power system. 4 gives simple operation.

Control of a multiphase output using a single phase reference requires some inertia of the "flywheel" synchronising circuit if the output is to be regular, and inertia is also used in some methods for maintaining output frequency in case of supply reference failure. Such inertia is gained in simple control loops at the expense of control response speed.

With systems employing a ring counter, the ability to programme the output sequence constitutes a degree of phase control.

In the present pulse generator a closed control loop is used to synchronise the pulse generator to the supply and a single phase reference is used. A low pass filter is incorporated to control transient response so that output regularity is adequate throughout each supply cycle. The pulse generator may be used in the frequency controlled mode, and exploratory trials may be made with asynchronous running; false lock may also be demonstrated.

Wide control range is provided to facilitate exploratory trials and the supply reference is processed so as to give satisfactory operation with a wide variety of supply voltage waveforms and frequencies.

Injection of the control signal into the control loop is performed in a passive loop filter so as to give smooth control over a wide range in any of the 3 basic operating modes (synchronised, false lock, frequency controlled) according to whether the supply reference is applied and depending on initial and subsequent control settings.

Digital detection of output phase gives freedom from waveform dependence, d.c. analogue control input gives simple circuitry, low-pass filtration of the sum of the above signals gives freedom from frequency dependence. Low pass filtration is used to ensure nearly equal conduction angles in all output phases, but finite inequality does exist; use of digital control signal could give perfect regularity together with almost instantaneous control

response, but special arrangements would have to be made to ensure that the control digit plus the phase difference digit produces a perfectly smooth sum for clock pulse generator control. Accommodation of variations in supply frequency would be another complication. Active (i.e. self adaptive) adjustment to give a smooth digit sum would automatically give accommodation of supply frequency variation.

5.11 Output Characteristics

Current and voltage availability of the power source, and current and voltage requirements of the thyristors determine the output characteristics of the pulse generator.

Resistors and transistors are the circuit elements which may be used to control the output characteristics of the unit. Instantaneous v-i characteristics may be resistive if series resistance is used in the output circuit, with the output and series resistance switched across the constant voltage d.c. supply, or a rectangular characteristic may be produced using a transistor in the common base mode, the emitter being fed with constant current via a resistor fed from a fixed fraction of the supply voltage.

The switched resistor is used in the present pulse generator; this gives an output characteristic with nearly uniform clearance over a wide range from the thyristor maximum gate power rating. The transistor current-source, voltage-limited approach fits the (I_{GT}, V_{GT}) locus better and is therefore suited to marginal firing; in this case power is dissipated in both transistor and resistor, to the detriment of such factors as cost, speed and size.

With ideal isolation and coupling, the static v-i characteristic would also apply with time-varying thyristor gate impedance. Distributed impedance in the coupling circuit makes application of a pulse having a time-invariant v-i characteristic impossible. Transmission line transformer and feeder techniques are difficult to apply because of the non-linear thyristor gate input impedance; this depends on anode and gate current history.

5.12 Cost

The cost of components used in the present pulse generator is given in table 5.12. Cost influences design because factors such as switching speed, power rating and amplification can be improved usually at the expense of one another or at increased cost. Current amplification and power dissipation are generally performed by transistors and resistors respectively, the transistors being used in the switching mode, therefore not absorbing appreciable amounts of power. High speed diodes, and also diodes with maximum current and voltage ratings in excess of thyristor gate pulse magnitudes, are considerably cheaper than diodes combining all of these qualities simultaneously.

		SUPPLY VOLTAGE DIVIDER	CLOCK PULSE GENERATOR	RING COUNTER	SHORT PULSE TIMER	SHORT PULSE GENERATORS	LONG PULSE GENERATORS AND ISOLATORS	INVERSION SWITCH	PHASE CONTROL	TOTAL NUMBER	COMPONENT COST	CIRCUIT COST
RESISTORS	1/2W.±5%	9	13	48	13	48	120	34	16	301	10/- PER 100	1 10 0
	PRE-SET				1					1	1 3	1 3
DIODES	HG1087			25	1	60		2	2	89	10	3 14 2
	1S923	2	1		1	48	48	3	5	109	1 8	9 1 8
	1S2051A								1	1	3 3	3 3
TRANSISTORS	2N3702	2	3	8	4	12	24	7	1	61	2 8	8 2 8
	2N3704	1	3			12		5	3	24	2 10	3 8 0
	TIP14	1								1	18 6	18 6
CAPACITORS	SMALL		1	8	1			3	3	16	6	8 0
	ELECTROLYTIC								2	2	1 6	3 0
MAGNETIC CORES						12	12		1	25	2 6	3 2 6
3-POLE, 2-WAY SWITCH				1						1	7 0	7 0
SUPPLY DECOUPLING CAPACITORS, ELECTROLYTIC										3	1 8	5 0
S.R.B.F. INSULATING BOARD												1 10 0
PINS											£2 PER 1000	2 0 0
TOTAL												34 15 0

TABLE 5.12

CHAPTER 6

CONCLUSIONS

Digital techniques may be used to generate thyristor gate signals of excellent quality with low cost of components. Digital circuitry may easily be tailored to meet special requirements such as frequency control and flywheel synchronisation.

Carrier frequency isolation of digital signals may be performed using a small number of active devices common to many output channels; this may be more economical than conventional techniques in which many active devices are used.

FUTURE WORK

This will consist of the design of digital pulse generators to suit particular thyristor inversion systems; many variations of control methods are possible, of which only 2 have been used in the present work. Output pulse quality may be improved in respect of

1. the abrupt termination of the firing pulse
2. the gaps present in the isolated holding pulse waveform.

It is suspected that 1 gives rise momentarily to reverse displacement current in the thyristor gate, which removes a small charge, tending to turn the thyristor off. This tendency will be increased by the reverse recovery of the short pulse rectifier,

which allows a small reverse gate current to flow at pulse termination. Derivation of firing and holding pulses from a single digit of long duration using pulse shaping techniques will reduce this effect.

2 gives rise to marginal firing where the single phase carrier is used to isolate firing pulses; the development of a multiphase carrier technique for isolation of digits with minimum distortion should prove interesting.

ACKNOWLEDGEMENTS

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Thanks are also due to Mr. C. Pratt, Mr. R. Auchinleck and Mr. R. McCullagh for permission to include material from their honours project reports.

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APPENDIX 1

FILTER TRANSFER RESISTANCE

With open circuit output,

$$\text{filter output voltage} = v_1 + \frac{(v_2 - v_1) R_1}{R_1 + R_2}$$

$$\text{filter output resistance} = R_3 + \frac{R_1 R_2}{R_1 + R_2}$$

$\therefore$ filter short-circuit output current

$$i_o = \frac{v_1 + \dfrac{(v_2 - v_1) R_1}{R_1 + R_2}}{R_3 + \dfrac{R_1 R_2}{R_1 + R_2}}$$

$$= \frac{v_1 R_1 + v_1 R_2 + v_2 R_1 - v_1 R_1}{R_3 R_1 + R_3 R_2 + R_1 R_2}$$

$$= \frac{v_1 R_2 + v_2 R_1}{R_1 R_2 + R_2 R_3 + R_3 R_1}$$

$$= A v_1 + B v_2$$

where $A = R_2/(R_1 R_2 + R_2 R_3 + R_3 R_1)$

$B = R_1/(R_1 R_2 + R_2 R_3 + R_3 R_1)$

APPENDIX 2

DYNAMIC RESPONSE OF PHASE CONTROL LOOP

The loop consists of a phase detector, a low-pass filter and a current-controlled pulse generator, Fig.A.2(a). The input voltage has phase θ_i, and the pulse generator output voltage has phase θ_o. When the loop is locked, phase detector output voltage $v_d = K_d(\theta_i - \theta_o)$ where K_d is the phase detector constant.

The phase control signal v_c is added to v_d and the sum filtered by the low-pass loop filter. This unit helps to determine the dynamic performance of the loop, and has transfer function $F(s) = K_F / (1 + sT_F)$. Terms containing v_c have been omitted to simplify analysis; this input was held constant in some tests and was a step function in others. The analysis gives system resonant frequency and damping factor, which are sufficient to indicate the nature of the transient response.

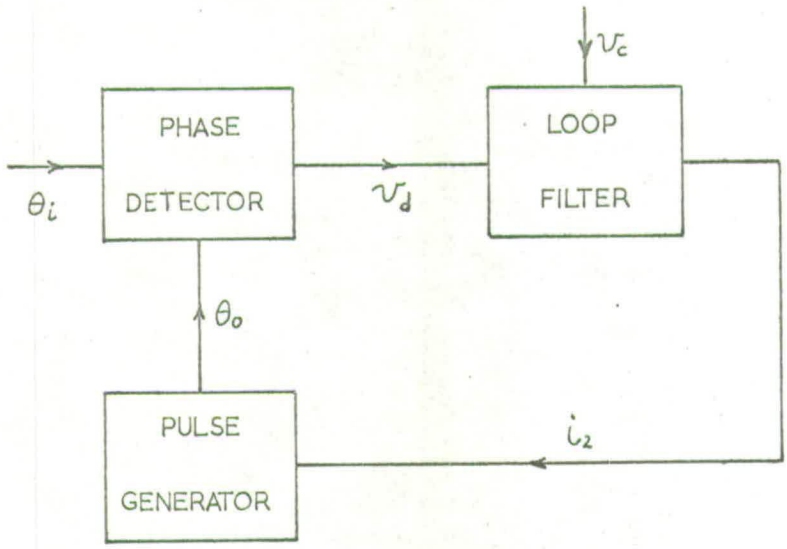
Pulse generator output frequency $f = \frac{d\theta_o}{dt} = K_o i_2$.

The following equations are applicable:

$$v_d = K_d(\theta_i - \theta_o) \qquad \text{(phase detector)}$$

$$i_2 = \frac{K_F\, v_d}{1 + sT_F} \qquad \text{(filter)}$$

$$\frac{d\theta_o}{dt} = K_o i_2 \qquad \text{(pulse generator)}$$



A.2(a)

K (calculated)	65	65	130	130	130	65	65	SEC^{-1}
T_F "	0·1	0·4	0·1	0·2	0·05	0·1	4·0	SEC
T "	·246	·493	·174	·246	·121	·246	1·56	SEC
ζ "	·196	·098	·138	·098	·196	·196	·031	
T (measured)	·28	0·4	·15	·22	·14	·28	2·0	SEC
ζ "	·22	·175	·175	·175	·175	·175	·05	
oscillogram fig. 3.4.1	(a)	(b)	(c)	(d)	(e)	(f)	(g)	(h)

A.2(b)

The loop equation is

$$s\theta_o = \frac{K_d K_F K_o(\theta_i - \theta_o)}{1 + sT_F}$$

putting $K = K_d K_F K_o$,

$$s\theta_o + \frac{K\theta_o}{1+sT_F} = \frac{K\theta_i}{1+sT_F}$$

The loop transfer function $H(s) = \frac{\theta_o}{\theta_i}$

$$= \frac{K}{(1+sT_F)(s + \frac{K}{1+sT_F})} = \frac{K}{s(1 + sT_F) + K}$$

$$= \frac{K}{s^2T_F + s + K} = \frac{K/T_F}{s^2 + s/T_F + K/T_F}$$

$$= \frac{\omega_o^2}{s^2 + 2\zeta\omega_o s + \omega_o^2}$$

where $\omega_o = \sqrt{\frac{K}{T_F}}$ and $2\zeta\sqrt{\frac{K}{T_F}} = \frac{1}{T_F}$ $\therefore \zeta = \frac{1}{2\sqrt{KT_F}}$

Values of T and ζ were obtained by calculation and measurement for various combinations of loop gain K and filter time constant T_F and the results tabulated, Fig.A.2(b).

Loop gain was increased to twice the original value by halving the impedance of all filter components, thereby doubling filter transfer admittance. The increased mean value of i_2 was counterbalanced by connection of a resistor to conduct the extra current to the -6V supply line.

Changes of filter time constant were made by alteration of filter capacitance only.

Values for K_o and K_d used in the calculation are 2,420 radians sec^{-1} mA^{-1} and 0.8075 volts $radian^{-1}$ respectively, from the calibration curves given in chapter 3. K_F was 1/30 mA $volt^{-1}$, calculated from the component values given in chapter 2, and this figure was doubled for some tests. T_F was 0.1 sec with original component values.

Multiplication of the above figures gives

loop gain $K = \frac{2{,}420 \times 10^3 \times 0.8075}{30} = 65.2$

oscillatory period $T = \frac{2\pi}{\omega_o} = 2\pi\sqrt{\frac{T_F}{K}} = 0.246$ seconds

damping ratio $\zeta = 0.1245$